A low-power, low phase noise CMOS VCO with suppression of 1/f flicker noise up-conversion

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Abstract: This paper proposes a low-power, low close-in phase-noise voltage-controlled oscillator (VCO) based on Colpitts oscillator. The VCO stacks the Colpitts VCO with a negative conductance cell. By exploiting a bias-level shifting technique, the proposed VCO provides larger output swing, and the close-in phase noise characteristics is improved impressively while consuming very low power. The proposed VCO is designed and simulated in 65 nm CMOS technology operating at 2.6 GHz with only 0.12 mA core current consumption from 0.5 V supply voltage. The simulated phase noise of the proposed VCO is $-27.6$ dBc/Hz at 100 Hz offset, $-54.4$ dBc/Hz at 1 kHz offset, and $-117.7$ dBc/Hz at 1 MHz offset frequency, respectively. The calculated figure of merit (FOM) is about $-198$ dBc/Hz at 1 MHz offset. Compared to that of the conventional VCO, the phase noise performance is significantly improved by more than 20 dB from 100 Hz to 1 kHz offset, around 15 dB at 10 kHz offset, and 6 dB at 1 MHz offset frequency, respectively.

Keywords: bias level shifting, CMOS, close-in phase noise, flicker noise, low-power, voltage-controlled oscillator

Classification: Integrated circuits

References

1 Introduction

The challenge in the design of an integrated CMOS voltage-controlled oscillator (VCO) is to achieve a low phase noise while dissipating low-power consumption. To reduce the power consumption, CMOS process scaling down has been done to drop the supply voltage. With the scaling down of CMOS process, the VCO performance is degraded which is mainly due to the limited output voltage swing with the reduced supply voltage.

For the VCO, it has been known that the tail current source is the main contributor in the close-in phase-noise offset frequency region [1]. While removing the tail current source, the close-in phase noise performance can be greatly improved. However, the current source in the VCOs can not be easily removed since the bias condition is destabilized and the loaded quality factor is degraded [2]. The remaining close-in phase contribution comes from the cross-coupled switching transistors, which are typically sized with the minimum channel length for large tuning range. However, the scaling down of the CMOS technology typically degrades the $1/f$ flicker noise performance of the MOS devices, which more difficult to tackle with. Several methods have been reported to suppress the flicker noise up-conversion in the VCOs. The first method is to inserting resistors in series with source terminals or drain terminals [3]. The second method is to use a capacitive coupling [4]. The third method is to employing a resonant network for relaxation oscillation [5]. However, the methods have disadvantages like consuming voltage headroom, large die size, oscillation start-up, etc.

In this paper, a low-power low close-in phase noise VCO is proposed by stacking a Colpitts type VCO with a negative conductance ($g_m$) cell. The $g_m$ cell adopts a bias level shifting technique to substitute current sources for the low operation voltage below 1.0 V and reduce the phase noise [6]. In Section 2, the proposed circuit design issues are described in detail compared to other topologies. In Section 3, the simulation results of the proposed VCO
is explained, and finally Section 4 gives a conclusion.

2 Circuit design

To compare the proposed VCO performances, several VCO topologies are considered as shown in Fig. 1. Fig. 1(a) shows the conventional NMOS only cross-coupled VCO. It can be shown that the negative admittance is simply \(-g_m\). Since it includes a current source, the noise is up-converted to the output, and degrades the overall phase noise performance. A filtering technique at the second harmonic can improve the phase noise performance. The phase noise performance of the cross-coupled VCO can be optimized in the current-limited regime where the oscillation amplitude is proportional to the bias current. Fig. 1(b) shows the \(g_m\) boosted differential Colpitts VCO (Diff Colpitts VCO) which is connected differentially with two single-ended Colpitts VCO [7].

The small-signal input admittances of the single-ended Colpitts VCO and differential Colpitts VCO are given by, respectively

\[
\text{Re}(Y_{in,\text{Colpitts-VCO}}) = \frac{-g_m \omega^2 C_1 C_2}{g_m^2 + \omega^2 (C_1 + C_2)^2}.
\]  
\[ \tag{1} \]

\[
\text{Re}(Y_{in,\text{Diff-Colpitts-VCO}}) = \frac{-g_m \omega^2 C_1 C_2 (2 + C_2/C_1)}{g_m^2 + \omega^2 (C_1 + C_2)^2}.
\]  
\[ \tag{2} \]

From (1) and (2), the negative small-signal conductance is increased by \(1 + C_2/C_1\) compared to that of the conventional single-ended Colpitts VCO. Thus, lower power consumption is required to make a reliable start-up. Fig. 1(c) shows the switched-biasing VCO [8]. Since all the transistors

\[
\begin{align*}
\text{Re}(Y_{in,\text{Colpitts-VCO}}) &= \frac{-g_m \omega^2 C_1 C_2}{g_m^2 + \omega^2 (C_1 + C_2)^2}, \\
\text{Re}(Y_{in,\text{Diff-Colpitts-VCO}}) &= \frac{-g_m \omega^2 C_1 C_2 (2 + C_2/C_1)}{g_m^2 + \omega^2 (C_1 + C_2)^2}.
\end{align*}
\]

Fig. 1. (a) Cross-coupled VCO, (b) \(g_m\) boosted differential Colpitts VCO [7], (c) Switched-biasing VCO [8], and (d) Proposed VCO.
in this VCO topology are switched, it is expected to have lower flicker noise. It has been reported that the switched biasing VCO can improve the phase noise about 5–8 dB at 100 kHz and 1 kHz offset frequency compared to that of the conventional fixed bias VCO. As the transistors operate in the triode region for the most of the time period, the transistors contribute lower current flicker noise than the transistors which operate in the saturation region [8]. Fig. 1(d) shows the proposed VCO by modifying Fig. 1 (a) and Fig. 1 (b). By removing the current source and adding coupling capacitors in the cross-coupled VCO, the $g_{m}$ cell in the proposed VCO is constructed. The capacitors $C_1$, $C_2$ and parasitic gate-source capacitance of $M_2$ form a differential Colpitts VCO. The cross-coupled transistors, $M_2$, form a negative conductance cell through coupling capacitors, $C_2$. By adopting a voltage dividing and bias level shifting technique, the transistor $M_2$ does not degrade the loaded quality factor of the oscillator and thereby reduce the current source noise contribution [6].

Fig. 2. (a) Proposed VCO to create the negative input admittance, and (b) small-signal equivalent circuit.

Fig. 2 shows the small-signal equivalent circuit of the proposed VCO. From Fig. 2, the negative input admittance can be calculated including the parasitic capacitances at the gate and drain terminals of $M_2$. In Fig. 2 (b), the total capacitance, $C_2$, at the drain node of $M_2$ consists of the parasitic drain-source capacitance, $C_{ds2}$, in parallel with the equivalent capacitance $C_t$, where $C_t$ is defined as $C_{cpl}C_{gs2}/(C_{cpl} + C_{gs2})$.

$$C_2 = C_{ds2} + C_t$$

$$v_{g2} = -ixC_t/(j\omega C_2C_{gs2} - g_{m2}C_t)$$

$$-v_x = v_{g1} + (ix - g_{m2}v_{g2})/j\omega C_2$$

$$v_x = (ix - g_{m1}v_{g1})/j\omega C_1 + (ix - g_{m2}v_{g2})/j\omega C_2$$

$$Y_{in,New-VCO} = (-\omega^2C_1C_2 - g_{m1})/(A + j\omega B)$$

where the coefficients $A$ and $B$ are given, respectively, as follows,

$$A = g_{m1} - g_{m2}C_2 (g_{m1}g_{m2}C_1 - \omega^2C_1C_2C_{gs2})$$

$$B = \frac{g_{m2}^2C_2^2 + \omega^2C_2^2C_{gs2}^2}{g_{m1}^2C_1^2 + \omega^2C_2^2C_{gs2}^2}$$

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DOI: 10.1587/elex.9.1881

Received July 26, 2012

Accepted September 04, 2012

Published December 28, 2012
\[ B = C_2 + C_1 - \frac{g_m C_t (g_m C_2 C_{gs2} + g_m C_1 C_t)}{g_m^2 C_t^2 + \omega^2 C_2^2 C_{gs2}^2} \]  

Comparing (1), (7), (8), and (9), it can be verified that the proposed oscillator operates as a Colpitts VCO with increased negative conductance compared to that of the conventional Colpitts VCO.

### 3 Simulation results

To verify the proposed idea, the four VCO circuits based on Fig. 1 are designed in 65 nm CMOS technology for comparison. For a fair comparison, the tank inductors and varactors in the VCOs are all the same, and the transistors are sized to operate at the same 2.6 GHz oscillation frequency.

Fig. 3 (a) shows the phase noise performance from 100 Hz, 10 kHz, and 1 MHz offset frequency as a function of bias voltage. As shown in Fig. 3 (a), the conventional cross-coupled VCO has a minimized optimum phase noise point at the low bias voltage. The phase noise performance of the other three VCOs has a comparatively flat response with the bias current. As shown in Fig. 3 (b), the output voltage swing of the cross-coupled and differential Colpitts VCOs is proportional to the bias current. For these VCOs, a trade-off between the phase noise and output swing is necessary. The output voltage swing of the switched VCO and the proposed VCO is almost constant across the different bias voltage. So, the bias current can be set to reduce the power consumption while keeping the excellent phase noise performance. Since the required VCO single-ended output swing should be larger than 0.3 V to drive

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**Fig. 3.** (a) Simulated phase noise as a function of dc current, (b) output voltage swing as a function of dc current, (c) phase noise performance of the four VCOs, and (d) the tuning range.
the mixer switches sufficiently, the bias current is chosen to be about 0.12 mA for the four VCOs to compare the performances from 0.5 V supply voltage. As can be seen from Fig. 3(c), the phase noise performance of the proposed VCO is significantly improved, especially in the offset frequency range close to the oscillation frequency. The tuning range is plotted in Fig. 3(d). The tuning range of the cross-coupled VCO and differential Colpitts VCO, which employ a fixed biasing current source, shows some nonlinear characteristic with the tuning voltage. However, the tuning range of the switched VCO and the proposed VCO, which employs a switched biasing scheme, shows a linear tuning characteristic since the varactor tuning characteristic is linearized due to a large output voltage swing.

The phase noise performance of several VCOs can be characterized with the figure-of-merit (FOM) given by where $PN$ is the phase noise of the VCO, $f_c$ is the VCO oscillation frequency, $\Delta f$ is the offset frequency, and $P_{dc}$ is the power consumption normalized to 1 mW.

The calculated FOM of the proposed VCO is about $-198$ dBc/Hz at 1 MHz offset frequency. The phase noise is improved about 20 dB at the close-in offset frequency ($\sim 1$ kHz), and about 6 dB at the far-out offset frequency.

4 Conclusion

This paper proposes a low-power, low close-in phase noise voltage-controlled oscillator (VCO) based on Colpitts oscillator. The VCO stacks the Colpitts VCO with a negative conductance cell. By exploiting a bias-level shifting and switched biasing techniques, the proposed VCO is designed to have a large output swing and the lower close-in phase noise characteristics. The proposed VCO is designed and simulated in 65 nm CMOS technology operating at 2.6 GHz with only 0.12 mA core current consumption from 0.5 V supply voltage. The simulated phase noise of the proposed VCO is $-27.6$ dBc/Hz at 100 Hz offset, $-54.4$ dBc/Hz at 1 kHz offset, and $-117.7$ dBc/Hz at 1 MHz offset frequency, respectively. The calculated figure of merit (FOM) is about $-198$ dBc/Hz at 1 MHz offset. Compared to that of the conventional VCO, the phase noise performance is significantly improved by more than 20 dB from 100 Hz to 1 kHz offset, around 15 dB at 10 kHz offset, and 6 dB at 1 MHz offset frequency, respectively.

Acknowledgments

The research was supported by a grant from the Academic Research Program of Korea National University of Transportation in 2012. This work was supported in part by the National Science Foundation CAREER grant (ECCS-0845849), CDADIC, and the Korean Government (NRF-2011-220D00084).