A low-variation on-resistance CMOS sampling switch for high-speed high-performance applications

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Abstract: This paper presents a high-linear bootstrapped sampling switch for high-speed applications. The proposed switch utilizes bootstrapping technique of both NMOS and PMOS types simultaneously. Thus, results in a low-variation low-value on-resistance switch. Using this idea, the proposed switch considers reliability constraints, and operates in full-swing input range. Furthermore, it is suitable for standard n-well CMOS technology. Simulation results show that proposed switch achieves on-resistance variation of less than 4% through full-range input signal.

Keywords: constant on-resistance, reliability, bootstrapping technique, high-speed applications

Classification: Integrated circuits

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1 Introduction

Employing a high performance front-end track-and-hold (T/H) circuit is essential to improve the dynamic performance of a high-speed analog-to-digital converter (ADC). In high-speed applications in which the T/H circuit must work in higher speed, a great care must be taken in choosing and designing of the T/H circuit. For instance, in a time-interleaved ADC that contains M channels, each converter operates at f_S/M while the front-end T/H typically operates at the total sampling frequency, f_S [1]. In a simple structure, the T/H circuit includes a sampling switch and a capacitor which form a low-pass filter in the track-mode. The variation of sampling switch on-resistance (R_{on}) causes dependence of time-constant of T/H circuit on input signal and thus, produces harmonic distortion. The R_{on} variation also introduces frequency dependant nonlinearity error in the track-mode; especially in high frequency input signal, this nonlinear variation causes input-dependent phase shift and therefore affects linearity. This distortion is called the track-mode distortion [2]. In conventional bootstrapped sampling switch [3], this nonlinear signal-dependant variation is mainly due to the body effect. As a straightforward approach, scaling up of the aspect ratio (W/L) of bootstrapped switch can reduce the R_{on} variation but at the expense of increasing junction capacitance that needs larger bootstrap capacitance to alleviate charge sharing between bootstrap capacitance and the sampling switch. Considering of more power consumption due to the larger sampling capacitance, this is not a suitable method in high sampling rates. A reliable sampling switch in standard n-well CMOS technology with R_{on} variation of less than 5%, which is appropriate for high performance high-speed applications is proposed. In next Section, a background of previous reported bootstrapped switches is presented. The proposed switch is explained in Section 3. Simulation results are then shown in Section 4. Finally, conclusions are given in Section 5.

2 Background

Bootstrapping approach can be realized by charging of a capacitor in the hold phase and then utilizing it as a floating battery during the sampling

phase for charging the sampling switch such that its gate tracks its source with a nearly constant voltage ($\sim V_{DD}$). In order to avoid degrading the long-term performance of CMOS device, which probably occurs due to the gate-oxide breakdown, hot electron, and punch-through effects, the voltage between main terminals of device (i.e. V_{GS} , V_{GD} , and V_{DS}) must be kept within the supply voltage of that technology [3]. Because of the nature of bootstrapping technique and also the need for a charge pump circuit, the gate voltage of main switch and voltage of some paths exceeds V_{DD} . However, in the conventional bootstrapped circuit, this problem has been solved applying some modifications such as using a cascaded transistor.

Bootstrapping technique is not able to cancel non-linearity impact of R_{on} variation due to the body effect. So, several compensation techniques have been proposed [4, 5, 6, 7, 8]. In an n-well CMOS process, the direct connection of bulk to source [4] or bootstrapping of bulk terminal [5] during the sampling phase can only be realized with PMOS devices. Nonetheless, because of difference in parameters of NMOS and PMOS device ($\mu_n \approx 4 \times \mu_p$), given an R_{on} value, PMOS device requires more dimensions compared to NMOS one. In high-speed applications, this may be problematic since increasing aspect ratio introduces more errors such as charge injection. On the other hand, to ensure a correct performance, the time-constant of network should be low enough. Another approach is bootstrapping both NMOS and PMOS switches [6, 7, 8]. The circuit presented in [6] suffers from device reliability and is not suitable for rail-to-rail applications. In Fig. 2 in [6], the V_{SG} of $M9$ in sampling phase and V_{SG} of $M17$ in hold phase exceed their allowable limit and reach their worst case $2 \times V_{DD}$ when input voltage is V_{DD} . Since the gate of $M17$ does not track its source with a shifted voltage, it does not pass the rail-to-rail signal properly. The CMOS switch proposed in [7] limits the peak input voltage because of leakage currents and latch-up. Since the gate of PMOS bootstrapped switch experiences negative voltage during the sampling phase, leakage currents from source and drain terminals to the bulk of the NMOS transistor which have to pass this negative voltage, become critical. In [8], using a linearizing method applied to a CMOS switch results improvement of linearity of equivalent conductance. Although, compare to conventional one maximum absolute value voltage of the circuit is less, however, some switches suffer from excessive voltage between their terminals (e.g. M_{2n} , M_{7n} , M_{2p} , and M_{7p} in Fig. 2 in [8]). In addition, because of lower overdrive voltage the switch indicates higher R_{on} compare to conventional one.

3 The proposed bootstrapped switch

Bootstrapping of both NMOS and PMOS switches has the advantage of decreasing the R_{on} value as well as reducing the R_{on} variation. However, as explained in Section 2 some limitations are forced. This work proposes a new structure for bootstrapping of a CMOS switch considering reliability and rail-to-rail operation. The principle of bootstrapping a CMOS switch is shown in Fig. 1 (a) and (b). Here, switches M_N and M_P are the main

sampling switches. M_P is body effect compensated in the first order by connecting its bulk to source in sampling phase. Two floating batteries can be implemented by switch-capacitor structures. The gates of N-type and P-type switches track the input voltage with the functions $V_{in} + V_{DD}$ and $V_{in} - V_{DD}$, respectively. As a result, the equivalent switch's R_{on} is as follows:

$$R_{on-CMOS} = \frac{1}{\mu_n C_{ox} (\frac{W}{L})_n (V_{DD} - V_{Thn}) + \mu_p C_{ox} (\frac{W}{L})_p (V_{DD} - V_{Th0p})} \quad (1)$$

By increasing both N-type and P-type switch sizes, their R_{on} are reduced leading to less time-constant. On the other hand, this increase results in more voltage error due to the charge injection and clock feedthrough. So, there is a trade-off in choosing aspect ratios. Fig. 1 (c) shows the proposed CMOS bootstrapped switch. The N-type part of proposed switch can be originally found in [3]. Proper biasing of the P-type part is achieved using some useful nodes in the N-type part of the circuit, so that the proposed CMOS switch maintains reliability as well as proper operation in the rail-to-rail input range. The bootstrapped switch works with a single phase clock. In the hold phase Ckn , gate of M_N connects to ground through M_{N11} . At the same time, M_P is turned off across M_{P5} . In this phase, C_{BOOST1} and C_{BOOST2} charge to V_{DD} . Because the gate of M_P is driven by negative voltage

Fig. 1. CMOS bootstrapped switch (a) sampling phase (b) hold phase (c) proposed circuit.

($V_{in}-V_{DD}$), any switch cannot be placed in this path. So, C_{BOOST2} must be directly connected to M_P . To provide the charge of V_{DD} on C_{BOOST2} , node $N3$ reaches $2 \times V_{DD}$ by M_{P1} . C_1 , C_2 , M_{N1} , and M_{N2} form the conventional clock multiplier. C_{BOOST1} is charged across M_{N3} and M_{N4} . M_{N7} and M_{N9} isolate M_N from the boosting capacitor. During the sampling phase Ck , M_{N6} connects the gate terminal of M_{N7} to the floating battery; consequently, M_{N9} , M_{P3} , M_{P2} , M_N , and M_P turn on in a way that their V_{GS} values are fixed at V_{DD} . Actually, the V_{GS} is less than V_{DD} , because of parasitic capacitances at nodes GN and GP . In the proposed switch, adding M_{P2} plays two important roles: First, it avoids exceeding the V_{DS} of M_{P3} from V_{DD} . Second, M_P can be simply body effect compensated by connecting its bulk to the node $N4$. In the mean time, properly operation of M_{P2} and M_{P3} are assured by connecting their gates to the nodes $N1$ and GN , respectively. M_{P3} also can be implemented as a PMOS device with its gate connected to node GP [4]. Node $N4$ shorts the bulk of M_P to its source. Thus, the V_{Th} of transistor M_P becomes constant. In order to prevent punch-through, extra transistor M_{N10} (M_{P4}) prevents the V_{DS} and V_{GD} of M_{N11} (M_{P5}) exceed from V_{DD} . Also, in order to avoid latch-up, bulk and source terminals of M_{N7} and M_{P1} are shorted. Note that at the beginning of sampling phase, M_{N7} , M_{N9} , and C_{BOOST1} are responsible for rising time of M_N . Similarly, M_{P2} , M_{P3} , and C_{BOOST2} directly affect the rise time of M_P . Proper aspect ratio values will result in equal time-constants. Another issue is related to the fall time of M_N and M_P . Any delay between turning off time of main switches leads to error in sampling capacitor and causes distortion. Consequently, a proper sizing of M_{N10} , M_{N11} , M_{P4} , and M_{P5} is necessary. The proposed switch considers reliability because none of V_{GS} , V_{GD} , or V_{DS} values of switches exceed V_{DD} even at presence of rail-to-rail input signal.

4 Simulation results

Both conventional [3] and proposed bootstrapped switch are simulated in a standard $0.18 \mu\text{m}$ CMOS technology model using Hspice simulator. A correct sizing of aspect ratios results in desired linearity; this can be achieved when both N-type and P-type switches have equal R_{on} values at the input common-mode voltage. In this design, $(W/L)_n = 5/0.18$ and $(W/L)_p = 21/0.18$ for proposed switch and its equivalent value for conventional one $(W/L)_n = 9.2/0.18$ is chosen. Fig. 2 (a) shows R_{on} value versus input signal amplitude. As can be seen, the proposed switch shows less R_{on} variation. This variation is only $\sim 3.5\%$ in proposed switch, whereas in conventional one is 24% . Dynamic performance comparison is achieved using a differential T/H circuit that includes two sampling switches and loading capacitors of 1 pF . A $1 V_{pp}$ sinusoidal signal, 500 MHz sampling clock, and 1.8 V supply voltage is applied to the circuits. SFDR plots of output versus input frequency from low to nyquist frequencies is shown in Fig. 2 (b). In high frequencies proposed switch shows more improvement where in near of nyquist frequency we have 13 dB improvement. Fig. 2 (c) presents SFDR results at different signal amplitudes

Fig. 2. Simulation results. (a) R_{on} variation against input signal amplitude (b) SFDR of fully-differential T/H circuits versus input signal frequency (c) SFDR plots for 250 MHz input frequency at different signal amplitudes (d) SFDR results versus different sampling frequencies with their equivalent nyquist input frequencies.

in 250 MHz input frequency. The simulation result shows 15 dB SFDR improvement for $1.8 V_{pp}$ input signal in proposed switch versus convention one. In Fig. 2 (d), the SFDR plots are shown versus different sampling frequencies with their equivalent nyquist input frequencies. Simulation result shows that at different sampling frequencies the proposed switch indicates SFDR more than 73 dB whereas SFDR of conventional one decreases to 61 dB at 500 MHz sampling rate. Table I confirms that remarkable improvement for reliability, rail-to-rail operation, and dynamic performance are achieved comparing to other CMOS switches. Note that some linearizing techniques such as bottom plate sampling and/or dummy switch is so effective in further dynamic

Table I. Comparison of CMOS bootstrapped switches.

CMOS bootstrapped switches	Max $ V_{GS} $, $ V_{GD} $, or $ V_{DS} $	Rail-to-rail operation	SFDR @ $1V_{pp}$, 246 MHz input
[6]	$2 \times V_{DD}$	No	67 dB
[7]	$3/2 \times V_{DD}$	No	57 dB
[8]	$V_{DD} + V_{th}$	Yes	71 dB
Proposed	V_{DD}	Yes	74 dB

performance improvement of switches especially at low frequency values.

5 Conclusion

Bootstrapping of both NMOS and PMOS switches have the advantage of both reducing the value of R_{on} and its variation. Using the above dual channel method a high-resolution reliable full-swing switch suitable for standard n-well CMOS technology is proposed. Simulation results indicate the effectiveness of proposed switch in high-speed applications.

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