Theoretical estimation of distorting effects by $t_{rr}$ of parasitic MOSFET-Diode in DCI-NPC audio power amplifiers

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Abstract: One of the topologies that can work at high Power and high Quality simultaneously is the DCI-NPC topology. This new topology has new parts and presents new voltage and distortion errors. One of these new elements are the MOSFET parasitic Diodes. These Parasitic-Diodes presents a Recovery Reverse Time ($t_{rr}$) and its distorting effects generates signal and quality losses, and EMI problems. These phenomena are introduced, modeled, studied and evaluated to discuss the affectation importance of the Recovery Reverse Time value in the Multilevel Power Amplifiers performance.

Keywords: power sound amplifiers, multilevel converters, EMI reduction

Classification: Electron devices, circuits, and systems

References

1 Introduction

Currently, the Class-D switching Amplifiers represent the most efficient sound amplifiers. For High Power Acoustics applications (Performances, Public address system), it is more important the efficiency than the sound quality, which allows working at lower switching frequencies. On the contrary, in High Quality applications (HiFi, Professional and Domestic Sound), the quality is the important fact and not the efficiency. An amplifier topology that would allow working at high power and high-quality sound would mean a breakthrough in the world of the Sound Switching Amplification. Multi-level DCI-NPC (Diode Clamped Inverter-Neutral Point Clamped) systems allow working at concurrent power and quality. Figure 1 shows a Full-Bridge DCI-NPC Topology [1, 2]. These converters are characterized by generating output signals of more than two levels of voltage output, thus increasing the quality of the output signal. The use of switching topologies in Power Audio Amplifiers, however, creates the appearance of new distortions [3]. High Frequency Distortions are not controllable and only can be minimized by using an optimal design.

![Diode-Clamped-Inverter or Neutral-Point-Clamped (DCI-NPC) Multilevel Topology with D\textsubscript{T1}D\textsubscript{T2}D\textsubscript{T3}D\textsubscript{T4} and D\textsubscript{T1'}D\textsubscript{T2'}D\textsubscript{T3'}D\textsubscript{T4'} Parasitic Diodes.](image)

Fig. 1. Diode-Clamped-Inverter or Neutral-Point-Clamped (DCI-NPC) Multilevel Topology with D\textsubscript{T1}D\textsubscript{T2}D\textsubscript{T3}D\textsubscript{T4} and D\textsubscript{T1'}D\textsubscript{T2'}D\textsubscript{T3'}D\textsubscript{T4'} Parasitic Diodes.

One of the most important High-Frequency Errors-Source is the reverse recovery time or t\textsubscript{rr} of the MOSFET diodes [3]. These effects are translated into short-circuits of short duration, and therefore into little dead zones or zero voltage output. These short-circuit cause an attenuation of the average value of output voltage, but in this case therefore their effects, only act during the circulation of reactive currents. Figure 1 show the DCI-NPC Topology with Parasitic MOSFET-Diodes.

2 Genesis of the distorting parasitic diodes t\textsubscript{rr}-error

The Parasitic Diode effects are the subject of some study recommendations made by experts in the matter in scientific and technical publications [4]. Is therefore a critical source of error and shortly analyzed in the view of experts in the field of switching amplifiers. The problem lies in the fact that
once have circulated reactive power, the MOSFET diodes keep in reverse circulation during an approximate time \( t_{rr} \), and therefore, in short-circuit drain-source of the MOSFET [5].

If this state coincides with the switching - ON of the other switch of the same branch (in the case of a typical Class-D topology) it will cause short-circuit of the DC-Link. In the case of DCI-NPC topology this problem has an added complication of having several states and hence, different combinations in the amplifier circuit. For each state of the system, the output voltage affected by the effects of the \( t_{rr} \) of the MOSFET diodes is different, which makes necessary to divide the study and the problem in two stages. The first scenario is defined by the existence of middle states and zero states in the output voltage. The second scenario corresponds to the application of mid and high/low states. In the first case, the amplifier is modulating a signal corresponding to an average output voltage \([0 \text{V} - (\pm V_{DC}/2)]\), in the second case, the system modulates in order to achieve voltages in the range of \([\pm V_{DC}/2] - (\pm V_{DC})]\). In the first of the scenarios, if the existence of a range of reactive conduction is supposed, the zero states and the double middle states keep alternating. Figure 2 (Top) shows a sequence corresponding to the switching of the positive half period for first scenario. In a positive half-period where the current has not achieved a positive value, there is alternation between the reactive middle-states with the current circulation trough \( D_{1'}T_{2'} - D_{T1}D_{T2} \) and the zero states with \( D_{1'}T_{2'} - T_{3}D_{2} \) and the short-circuit produced in \( D_{T1(Trr)}D_{T2(Trr)} - T_{3}D_{2} \) because of the reverse recovery of the diodes in switches \( T_{1} \) and \( T_{2} \). During the application of the other combination of reactive half-positive \( D_{T4'}D_{T3'} - T_{3}D_{2} \) with which during the following switching to the zero-state \( D_{1'}T_{2'} - T_{3}D_{2} \) the short-circuit will be produced through \( D_{1'}T_{2'} - D_{T3(Trr)}D_{T4(Trr)} \). This sequence will keep repeating while the current keep its reactive state. In both cases, the short-circuit that is produced is the one of on DC-Bus capacitor, and therefore of an absolute value of \( V_{DC}/2 \). The lasting of this scenario is fixed by the reactive angle \( \varphi^\circ \), and taking in account that the total lasting of the modulating interval zeros-middle is:

\[
\lambda^\circ = 2 \cdot \left[ \sin^{-1} \left( \frac{0.5}{m} \right) \right] \quad \text{where} \quad m = \frac{V_{OUT}}{V_{DC}} \quad \text{or} \quad \text{Modulation Index} \quad (1)
\]

In the second scenario, if it is supposed the existence of an interval of reactive conduction, and it remains to part of the interval of the figure 2 (Bottom), the high/low states alternate with double middle-states, so for a positive half-period where the current still has not achieved a positive value, reactive half-positive states and current circulation through \( D_{1'}T_{2'} - D_{T1}D_{T2} \) alternate, and so do high states with \( D_{T4'}D_{T3'} - D_{T2}D_{T1} \) and the short-circuit that is produced in \( D_{T1(Trr)}D_{T2(Trr)} - T_{3}D_{2} \) because of the reverse recovery in the diodes of switches \( T_{1'} \) and \( T_{2'} \). During the application of the other combination of reactive half-positive \( D_{T4'}D_{T3'} - T_{3}D_{2} \) with which during the following switching to the high-state \( D_{T4'}D_{T3'} - D_{T2}D_{T1} \) the short-circuit will be produced through \( D_{1'}T_{2'} - D_{T3(Trr)}D_{T4(Trr)} \). This sequence will keep
repeating while the current keep its reactive state. In both cases, the shortcircuit that is produced is the one of the two DC-Bus capacitors, and therefore of an absolute value of \( V_{DC}/2 \). The lasting of this scenario is fixed by the reactive angle \( \varphi^o - \lambda^o \), and taking in account that the total lasting of the modulating interval high/low states and middle-states is:

\[
\beta^o = \left\lfloor \tan^{-1}\left(\frac{W_{IN} \cdot L_Z}{R_Z}\right) \right\rfloor - \left\lfloor \sin^{-1}\left(\frac{0.5}{m}\right) \right\rfloor
\]

\( 0^o < \varphi_z < \left\lfloor \sin^{-1}\left(\frac{0.5}{m}\right) \right\rfloor \)  

\( \lambda = \left[ \sin^{-1}\left(\frac{0.5}{m}\right) \right] \)  

\( \varphi_z = \left\lfloor \tan^{-1}\left(\frac{W_{IN} \cdot L_Z}{R_Z}\right) \right\rfloor - \left\lfloor \sin^{-1}\left(\frac{0.5}{m}\right) \right\rfloor \)  

\( \beta = \left\lfloor \tan^{-1}\left(\frac{W_{IN} \cdot L_Z}{R_Z}\right) \right\rfloor - \left\lfloor \sin^{-1}\left(\frac{0.5}{m}\right) \right\rfloor \)  

\( 0^o < \varphi_z < \pi - \sin^{-1}\left(\frac{0.5}{m}\right) \)  

Fig. 2. (Top) MOSFET-Diodes \( t_{rr} \)-Error in Positive Half-Period Switching for Neutral - Middle States Operation. (Bottom) MOSFET-Diodes \( t_{rr} \)-Error in Positive Half-Period Switching Operation for Middle - Top States Operation.
Where $W_{IN}$ [rad/s] is the input signal frequency, $L_Z$ [H] and $R_Z$ [Ω] are the Inductive and Resistive values of the Load.

### 3 Model and evaluation of $t_{rr}$-error

The error $\varepsilon V_{OUT}$ produced by the clamped diodes can be expressed in average value as:

$$\varepsilon V_{OUT(t_{rr},T_{SW})} \simeq -2 \cdot \frac{V_{DC}}{2} \cdot (t_{rr} \cdot f_{SW}) \cdot \alpha_{PND}$$

(3)

Where $\alpha_{PND}$ is the weighting factor of the error and is directly depending on the different angles of applications of reactive states:

$$\alpha_{PND} = \left[ \tan^{-1} \left( \frac{W_{IN} \cdot L_Z}{R_Z} \right) \right] - \sin^{-1} \left( \frac{0.5}{m} \right) + \left[ \sin^{-1} \left( \frac{0.5}{m} \right) \right]$$

(4)

The factor $\alpha_{t_{rr}}$ indicates the proportion between the existence time of the perturbation generated during the $t_{rr}$, and the total modulation period $(T_{SW})$.

$$\alpha_{t_{rr}} = \frac{t_{rr}}{T_{SW}}$$

(5)

In order to analyze the amplitude error generated by the effects of the $t_{rr}$ of the MOSFET diodes, some multiparameter simulations have been performed, where it has been evaluated this error as a function of one reactive interval $\omega L/R = [0.01, 0.6, 1, 10]$, where 0.01 corresponds to an almost resistive charge and therefore a reactive current almost null, and 10 corresponds to an almost inductive charge with a big angle lag of voltage-current. This variation of charge has been simulated using different times $t_{rr}$ and switching frequencies. These parameters have been related by the factor $\alpha_{t_{rr}}$ (5). the remaining operating conditions are $V_{DC} = 100$ V, $f_{IN} = 1$ kHz. Figure 3 (Top) shows the results of the multiparameter evaluation of the error generated by the $t_{rr}$ of the MOSFET diodes. To analyze the effects of the reverse recovery time of the MOSFET diode in the THD of the amplitude error $\varepsilon THD(t_{rr}, T_{SW})$, the following expression can be used with the weighting factor $\alpha_{PND}$.

Transforming the expression (3) in the frequency domain, the error $\varepsilon V_{OUT}$ can be expressed as a series of harmonic components such that:

$$\varepsilon V_{OUT(\alpha_{t_{rr}},f_{SW})} \simeq -2 \cdot \alpha_{t_{rr}} \cdot \alpha_{PND} \cdot \frac{V_{DC}}{2} \cdot \sin \left( \frac{n \cdot \pi}{2} \right)$$

(6)

With which the $\varepsilon THD$ is expressed as:

$$THD_{\varepsilon V_{OUT(\alpha_{t_{rr}},f_{SW},m)}} \cong \left( \sum_{i=2}^{i=M_{MAX}} \left[ -2 \cdot \alpha_{t_{rr}} \cdot \alpha_{PND} \cdot \frac{V_{DC}}{2} \cdot \sin \left( \frac{n \cdot \pi}{2} \right) \right]^{2} \right)$$

$$\left( m \cdot \frac{V_{DC}}{2} - \alpha_{t_{rr}} \cdot \frac{4\pi}{2} \right)$$

(7)
Figure 3 (Left) shows the effects of the trr with respect to the quality of the spectrum of the εTHD(t_{rr}, T_{sw}) error, the conditions under which this error has been evaluated are those of t_{rr} = 100 ns and f_{SW} = 200 kHz (αt_{rr} = 20 m), m = 1, V_{DC} = 100 V and the load factor (ωL/R) = [0 – 10].

4 Conclusions

Figure 3 (Top) shows how, for very low inductive values, the current is fully active and therefore, the existence of reactive circulation and short-circuits generated by the t_{rr} is nonexistent. This error maintains its value below 0.6% for typical values of t_{rr} and f_{SW} (αt_{rr} = 20 m at t_{rr} < 100 ns, f_{SW} = 200 kHz) in switching amplifiers and typically electro-acoustic loads (ωL/R) < 10. In any case, the t_{rr} is not shown as a critical source of error, but should diminish its importance as the values of amplitude error εV_{OUT}(t_{rr}, T_{sw}) are very far from the regulatory threshold of 15%. However, it should be noted that these values so low are mainly due to the short time during which diodes perform. The effects of the t_{rr} in terms of distortion or εTHD(T_{rr}, T_{sw}) error, unlike in the case of the εV_{OUT}(T_{rr}, T_{sw}), have to be taken into consideration. As

Fig. 3. (Top) V_{OUT} Error for different Diode α_{t_{rr}} and ωL/R values. (Bottom) THD for different ωL/R values at α_{t_{rr}} = 20 m (t_{rr} = 100 ns, f_{SW} = 200 kHz).
shown in figure 3 (Bottom), above a load factor \(\omega L/R = 5\), the total THD exceeds the regulatory threshold of 1%. This value \(\omega L/R = 5\) corresponds to an electroacoustic load impedances of \(R_{LOAD} = 8 \, \Omega\) and \(L_{LOAD} = 32 \, \mu H\) for a \(f_{SW} = 200 \, kHz\).

Acknowledgments

This work was supported by Spanish Ministry of Science and Technology under the TRA 2010-21598-C02-01 Research project.