A PVT insensitive boosted charge transfer for high speed charge-domain pipelined ADCs

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Abstract: A process, voltage, temperature (PVT) insensitive boosted charge transfer (BCT) circuit for charge-domain (CD) pipelined analog-to-digital converters (ADC) is presented. The output charge of existing BCT varies extensively with PVT variation, leading to large common-mode charge errors in each differential BCT stage when used in CD pipelined ADCs. Therefore, complicate common-mode control circuits must be adopted to stabilize the common-mode charge of each stage, which consumes large power and chip area. The proposed BCT circuit employs a differential difference amplifier and a differential voltage reference to reject the charge errors caused by PVT variations. A 125-MSPS, 10-bit CD pipelined ADC without common-mode control circuit is implemented based on the proposed BCT, consuming only 27 mW from a 1.8 V supply.

Keywords: charge domain, pipelined ADC, charge transfer circuit

Classification: Integrated circuits

References

- [1] M. Anthony, E. Kohler, J. Kurtze, L. Kushner, and G. Sollner, "A process-scalable low-power charge-domain 13-bit pipeline ADC," *IEEE Symp. VLSI Circuits*, pp. 222–223, June 2008.
- [2] M. Anthony and G. Sollner, "Ultra-low-power 500-MSPS 12-bit A/D converter using interleaving and CMOS charge-domain technology," *Annual Compound Semiconductor Integrated Circuit Symposium*, pp. 1–4, Oct. 2009.
- [3] M. Yoshioka, M. Kudo, K. Gotoh, and Y. Watanabe, "A 10 b 125 MS/s 40 mW pipelined ADC in 0.18 μm CMOS," *ISSCC Dig. Tech. Papers*, pp. 282–283, 2005.
- [4] K.-H. Lee, S.-W. Lee, and Y.-J. Kim, "Ten-bit 100 MS/s 24.2 mW 0.8 mm² 0.18 μm CMOS pipeline ADC based on maximal circuit sharing schemes,"

- IET Electronics Letters*, vol. 45, no. 25, pp. 588–589, Dec. 2009.
- [5] J. Li and U. K. Moon, “A 1.8-V 67-mW 10-bit 100-MS/s pipelined ADC using time-shifted CDS technique,” *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1468–1476, Sept. 2004.

1 Introduction

The charge domain (CD) pipelined ADC based on boosted charge transfer (BCT) circuits is a newly emerging opamp-less ADC architecture [1, 2], which can achieve high speed A/D conversion at lower power dissipation compared with those conventional pipelined ADCs based on switched-capacitor architectures [3, 4, 5]. However, the output charge amount of the BCT in [1, 2] is influenced remarkably by process, voltage and temperature (PVT) variations, which can cause large fluctuations in the common-mode charge when the BCTs are used in CD pipelined ADCs. The common-mode charge errors reduce the input signal range of the ADC extensively. Furthermore, as common-mode charge error accumulates stage by stage, several stages at the backend of the pipeline may fail to function when common-mode charge error increases to a given extent. In order to solve the problem, complicated common-mode charge control techniques are introduced in [1, 2] to stabilize common-mode charge in each stage, which increases the design complexity, chip area and power consumption. This letter presents a new BCT that adopts a differential difference amplifier (DDA) with a differential voltage reference to reject the output common-mode charge errors caused by PVT variations. With the proposed BCT, common-mode charge control circuits can be eliminated in CD pipelined ADCs, and even lower chip area and power consumption can be achieved.

2 BCT circuits

2.1 Analysis of the existing BCT

The BCT circuit in [1] and its operating waveforms are given in Fig. 1 (a). The gate of M_S is controlled by the output of amplifier A_1 , which is composed of M_1 , M_2 and M_3 . Before t_1 , Φ_1 is in high state, and M_S is initially turned off. The source node (S) and the drain node (D) of M_S are set to reference voltages V_{p1} and V_{p2} , respectively. The input signal V_{in} is tracked and converted into charge by capacitor C_1 . The charge transferring process is initiated at t_1 when Φ_1 changes to low state and the voltage at node A, V_A , falls to ground through switch S_2 . The voltage change of V_A causes a voltage drop at node S (V_S), which in turn induces a larger increase in V_G because of amplifier A_1 . The large voltage difference between V_G and V_S turns on M_S . Due to the difference between V_D and V_S , charge stored on C_1 transfers onto C_2 , which causes V_S to rise and V_D to fall. Then, amplifier A_1 drives V_G to fall gradually. At time t_2 , when V_S settles to the cut-off value V_0 , M_S is turned off and the charge transfer process is terminated. At t_3 , the next

charge conversion and transferring process is started. The charge transferred in the whole process can be expressed in terms of the voltage change across capacitor C_1 ,

$$\begin{aligned} Q_T &= C_1 \cdot \{[V_A(t_2) - V_A(t_1)] - [V_S(t_2) - V_S(t_1)]\} \\ &= C_1 \cdot [-V_{in}(t_1) + V_{P1} - V_0], \end{aligned} \quad (1)$$

where V_0 is the voltage at node S when M_S is just turned off, which is determined both by the size and threshold voltage of M_S , and the input/output characteristics of amplifier A_1 . Under ideal PVT conditions, V_0 is almost a constant [1].

In CD pipelined ADCs, two BCTs are employed in a conversion stage to perform differential signal processing [1]. Assuming the input signals of the differential stage are V_{inp} and V_{inn} , the differential charge, $Q_{T,diff}$, and the common-mode charge, $Q_{T,CM}$, can be obtained from Eqn. (1):

$$\begin{aligned} Q_{T,diff} &= C_1 \cdot [V_{inp}(t_1) - V_{inn}(t_1)] \\ Q_{T,CM} &= C_1 \cdot [-V_{in,CM} + V_{P1}/2 - V_0/2] \end{aligned} \quad (2)$$

where $V_{in,CM} = (V_{inp} + V_{inn})/2$, is the common-mode level of the input differential voltage. From Eqn. (2), the differential output charge is a linear function of the differential input voltage at t_1 . Therefore, A/D conversion can be performed by quantization of the differential voltage at node D between t_1 and t_2 . Conditional charge subtracting (or adding) circuits are also needed at node D to form a complete CD pipeline stage [1], which are omitted in Fig. 1 for simplicity.

As shown in Eqn. (1), the common-mode charge is determined mainly by $V_{in,CM}$, V_{P1} , and V_0 . The input common-mode level, $V_{in,CM}$, can be set by off-chip common-mode circuit, and V_{P1} is often generated by a bandgap reference. Therefore, $V_{in,CM}$ and V_{P1} is relatively stable under PVT variations. However, because V_0 is mainly determined by the DC operating point of amplifier, A_1 , it will vary extensively with PVT and cause large common-mode charge errors.

2.2 The proposed PVT insensitive BCT

The proposed BCT structure and its operating waveforms is given in Fig. 1 (b), in which a DDA is used to detect the voltage difference between node D and node S, ($V_D - V_S$), and compare it with a differential reference $V_{r2} - V_{r1}$. The charge transferred can be expressed in term of the voltage change across C_1 or C_2 :

$$Q_T = C_1 \cdot \{[V_A(t_2) - V_A(t_1)] - [V_S(t_2) - V_S(t_1)]\} = C_2[V_D(t_2) - V_D(t_1)] \quad (3)$$

After t_2 , the DDA set $V_D - V_S$ towards $V_{r2} - V_{r1}$:

$$V_D(t_2) - V_S(t_2) = V_{r2} - V_{r1} \quad (4)$$

Applying Eqn. (4) into Eqn. (3) and substituting each voltage term with its corresponding value, the transferred charge can be recalculated as

$$Q_T = [-V_{in}(t_1) + (V_{p2} - V_{p1}) - (V_{r2} - V_{r1})] \cdot [C_1 C_2 / (C_1 + C_2)] \quad (5)$$

Fig. 1. BCTs and operation waveforms: (a) the BCT in [2]; (b) the proposed BCT; (c) the schematic and simulated waveform of the proposed BCT.

For a differential conversion stage composed of two proposed BCTs, the differential and common-mode charge can be expressed as

$$Q_{T,diff} = [V_{inp}(t_1) - V_{inn}(t_1)] \cdot [C_1 C_2 / (C_1 + C_2)]$$

$$Q_{T,CM} = [-V_{in,CM} + (V_{p1} - V_{p2})/2 - (V_{r2} - V_{r1})/2] \cdot [C_1 C_2 / (C_1 + C_2)] \quad (6)$$

From Eq. (6), $Q_{T,diff}$ is still a linear function of the differential input voltage at t_1 . However, comparing to Eq. (2), $Q_{T,CM}$ of the proposed circuits is mainly determined by $V_{in,CM}$ and the difference of two pair of reference voltages. Hence, it is more insensitive to PVT variations than that of BCT in Fig. 1 (a).

Circuit implementation of the proposed BCT is shown in Fig. 1(c), in which the input and output switch capacitor circuits are omitted for simplicity. Simulated transient waveforms of the proposed circuit with a clock

frequency of 125 MHz are given in Fig. 1(c). The charge transferring process is initiated at t_1 as discussed above. The DDA senses the large value of $V_D - V_S$ and turns on M_S . The value of $V_D - V_S$ reduces gradually and settles to $V_{r2} - V_{r1}$ at t_2 when V_G falls to a given low value and turns off M_S . The simulated settling time is about 2.6 ns, which means the proposed BCT can work under a clock frequency above 125 MHz.

3 Simulation and measurement results

The proposed BCT is designed with TSMC 0.18 μm CMOS technology, and simulated at a 1.8 V power supply. A sample circuit for the BCT in Fig. 1(a) is also designed for comparison. The capacitors and the transistor M_S of both BCTs are designed with the same sizes ($C_1 = 2 * C_2 = 1 \text{ pF}$, $(W/L)_{M_S} = 20 \mu/0.3 \mu$). The amplifier A_1 in Fig. 1(a) and the DDA in Fig. 1(c) are both designed with a gain of 30 dB. An equivalent charge expression is chosen for both BCTs to compare charge waveforms:

$$Q_e = (V_D - V_S) \cdot C_1 C_2 / (C_1 + C_2) \quad (7)$$

Fig. 2. Comparisons of simulation results under different conditions: (a) process corners; (b) supply voltages; (c) temperature.

The simulated Q_e under different process corners (SS for slow, TT for typical and FF for fast), temperatures, and supply voltages are given in Fig. 2.

As can be seen from Fig. 2, the charge waveforms of the BCT in Fig. 1 (a) vary significantly with large PVT variations, while the waveforms of proposed BCT keep almost unchanged, which verifies that the proposed BCT can reject charge errors due to PVT variations remarkably. The proposed BCT's power consumption is about twice of the conventional one. However, this power consumption increase is much smaller than the power consumption of common mode control circuit used in the conventional CD pipelined ADCs.

A 10-bit 125-MSPS CD pipelined ADC is designed and fabricated based on the proposed BCT without using any common mode charge control technique, with chip photo given in Fig. 3 (a). The chip area is $1.4 \times 1.0 \text{ mm}^2$. The measured FFT spectrum, DNL and INL curves are shown in Fig. 3 (b), (c) and (d), respectively. The prototype ADC achieves a SFDR of 67.7 dB, a SNDR of 57.3 dB, a DNL of 0.5 LSB, and an INL of 0.7 LSB with a 3.79-MHz sinusoid input signal at full sampling rate, consuming only 27 mW from a 1.8-V power supply.

Fig. 3. Die photograph and measured results of the prototype ADC: (1) die photograph; (b) FFT spectrum; (c) DNL curve; (d) INL curve.

4 Conclusion

This paper presents a PVT insensitive BCT for high speed CD pipelined ADCs. Simulation results show that the PVT variation rejection of the proposed circuit is much improved compared with existing BCTs. The proposed

BCT is verified by a 27 mW 10-bit 125-MSPS CD pipelined ADC without using any common mode charge control techniques.

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