A parasitic insensitive C-DAC with time-mode reference voltage generator

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Abstract: This paper proposes a 10-bit parasitic insensitive capacitive DAC with time-mode reference voltage generator for high resolution LCD drivers. In this architecture, the parasitic insensitive operation is achieved by modifying the switch control scheme of the DAC. Furthermore, the time-mode reference voltage generator replaces the conventional resistor divider scheme, which reduces the size of the reference generation circuitry and enables programmable DAC reference voltage. The proposed DAC was designed with CMOS 0.35 µm technology. The maximum INL and DNL showed −0.049 LSB and −0.026 LSB even with 10% parasitic capacitance.

Keywords: C-DAC, parasitic insensitivity, time mode reference generator

Classification: Integrated circuits

References

1 Introduction

Nowadays, image sources require high resolution, due to increasing display panel size, and higher demand for better image quality from the end users. Therefore, the digital-to-analog converter (DAC) which is an essential component in display driver must have high resolution [1, 2]. For higher resolution, capacitive-type DACs (C-DACs) are better than resistive-type DACs, since they lead to lower power consumption and area [3, 4]. However, as the resolution increases the performance of C-DACs are critically limited by parasitic capacitance, and the capacitor area is also a heavy burden. Although the double bit processing in single capacitor scheme [4] can considerably reduce the capacitor area, precise reference voltage generation using the resistor divider is still problematic.

In this paper, a parasitic insensitive 10-bit C-DAC with time-mode reference generator is proposed. Instead of generating the DAC reference voltages with the conventional resistor divider, the proposed DAC uses a time-mode reference voltage generator based on time-mode signal processing [5]. Although the proposed scheme is similar to [5], since both approaches use time difference variables as an intermediate way of processing the voltage signal, [5] mainly uses the delay difference whereas the proposed scheme varies the pulse width to generate different reference voltages, which is much simpler and can reduce the reference generator area.

2 Proposed parasitic insensitive DAC

Fig. 1 (a) shows the operation of the proposed DAC. The DAC architecture uses a similar double bit processing in single capacitor structure [4] to reduce the capacitor area, yet the switch control scheme is modified to achieve parasitic capacitance insensitive operation.

The detail switch configuration of the parasitic insensitive DAC is depicted in Fig. 1 (b), where $C_{P1}$ and $C_{P2}$ represent the top and bottom plate parasitic, respectively. For simplicity, only one capacitor $C$ is described. In addition, the feedback parasitic is not included, since this does not affect the DAC output voltage. During phase-1, in case $b_5$ is high, $C_{P1}$ will be charged to GND while $C_{P2}$ is charged to $V_{REF}$. In phase-2, $C_{P2}$ is connected to either $-V_{REF}/32$ or GND. However the charge stored in $C_{P1}$ will not change, since $C_{P1}$ is connected to the input node of the amplifier which is virtual GND. As a result, the charge stored in $C_{P2}$ will not transfer to the feedback capacitor $32C$ through $C$, since the bottom plate of $C$ is connected to a constant voltage, and $C_{P2}$ is not directly connected to $32C$. Therefore, $C_{P1}$ and $C_{P2}$ do not affect the output voltage of the DAC, which enables the parasitic insensitive operation.

3 Time-mode reference voltage generator

Although the proposed DAC is insensitive to parasitic capacitance, the accurate generation of the two reference voltages $V_{REF}$ and $-V_{REF}/32$ are still
Fig. 1. (a) Operation of the proposed parasitic insensitive 10-bit C-DAC (b) Detail switch configuration

problematic. Fig. 2(a) shows the conventional resistor divider reference generator, whereas Fig. 2(b) shows the proposed time-mode reference voltage generation circuit with the control clock timings. The time-mode reference generator occupies less area, since the resistor string is replaced with two capacitors and several control switches.

The proposed reference generator first charges capacitor $C_1$ until the voltage across $C_1$ reaches the desired reference voltage level $V_{REF}$ or $V_{REF}/32$, and transfers this charge to capacitor $C_2$. A reference current $I_{REF} = 16 \mu A$ was generated by setting $V_{in} = 1$ V and $R = 62.5 \, k\Omega$, since $I_{REF} = V_{in}/R$. The DAC reference voltages $V_{REF}$ and $V_{REF}/32$ are obtained by controlling the charging time of $C_1$, which is set by the pulse width of $T$. That is...
\[ V_{C1} = \frac{k \cdot I_{REF} \cdot T_d}{C_1} \]  

(1)

Where \( k \) is the current scaling factor and \( T_d \) is the pulse width. In order to minimize both the charging current and capacitor size, small \( k \) value is preferred, since this will enable reduced area and power consumption of the reference generator. The value of \( k \) is set by the size of the current mirror transistors \( M_2 \) and \( M_3 \). That is

\[ k = \frac{(W/L)_3}{(W/L)_2} \]  

(2)

where \( W \) and \( L \) are the width and length of the transistors. However, small \( k \) will make the charging current fall below the \( \mu A \) range which can degrade the current mirror matching that will eventually lead to reference voltage error. As a result, the optimum value of \( k \) was set to 1/8. This leads to a capacitor charging current of 2 \( \mu A \), and \( T_d \) of 160 ns and 5 ns for \( V_{REF} = 1 \text{V} \) and \( V_{REF/32} = 31.25 \text{mV} \), respectively with \( C_1 = C_2 = 320 \text{fF} \).

Furthermore, in each phase-1 (\( S_1 = H \)) and phase-2 (\( S_2 = H \)), \( C_1 \) is charged while \( C_2 \) is discharge during the first half, and \( C_1 \) is connected to \( C_2 \) via the reference amplifier during the remaining second half. Therefore, the output voltage of the reference amplifier \( V_R \) is set to \( V_{REF} \) in phase-1 and \( -V_{REF/32} \) in phase-2, where \( V_R \) is connected to the bottom plate of each capacitor \( C \sim 16C \) to supply the DAC reference voltage. However, during phase-2, the top plate of \( C_1 \) is connected to the input node of the reference amplifier to invert the polarity of the output voltage \( V_R \) that will lead to \( -V_{REF/32} \). The control clocks including \( C_1 \) charging pulse \( T \) and \( C_2 \) discharging pulse \( R \), and two non-overlapping clocks \( S_1 \) and \( S_2 \) are all generated from a 100 MHz main clock with 50% duty cycle. The pulse width \( T_d \) of 5 ns and 160 ns were obtained by combining the counter outputs that divide the frequency of the main clock with combination logics. With now-a-days CMOS technology, it is not difficult to generate control signals by processing a 100 MHz clock. However, in order to minimize the rise and fall time of the control signals, buffers were used to drive the following loads of the control clocks. In addition, with the 100 MHz clock, we expect the jitter is not critical than the rise and fall time, unless it is huge. The estimated area of the proposed reference generator compared to the conventional reference generator is 45%, which is less than half of the conventional circuit.

However, the proposed time-mode reference generator can limit the conversion speed of the DAC, since the reference voltage is determined by the absolute pulse width of the control signal (160 ns for \( V_{REF} \) and 5 ns for \( V_{REF/32} \)), and requires an extra cycle for discharging \( C_2 \). Therefore, it is beneficial to adopt the proposed scheme for low speed applications such as the DAC used for high resolution and compact mobile LCD display driver ICs. In addition, accurate generation of the control signal pulse width can be another drawback, since this can add extra circuitry and power to minimize the rise and fall time.
4 Simulation results

The proposed DAC including the time-mode reference voltage generator was designed using CMOS 0.35 µm technology with supply voltage of 3.3 V. A 2-stage amplifier was used for the DAC main amplifier, and a folded-cascode amplifier was used for the reference amplifier. Furthermore, the value of the unit capacitor (C) was set to 100 fF. The DAC was able to operate with conversion rate up to 1.5 MS/s.

Fig. 3 (a) and 3 (b) show the INL and DNL plots of the conventional C-DAC [4] with 1% top and bottom plate parasitic capacitances. Fig. 3 (c) and 3 (d) show the INL and DNL plot of the proposed DAC with 10% top and bottom plate parasitic. For the conventional DAC, the maximum INL and DNL are around 10.1LSB and 1.02LSB with 1% top and bottom plate parasitic capacitances. The maximum INL and DNL of the proposed DAC are around $-0.049\text{LSB}$ and $-0.026\text{LSB}$ even with 10% top and bottom plate parasitic capacitances. This shows the parasitic insensitivity and proper operation of the time-mode reference voltage generator.

The reference current $I_{\text{REF}}$ change due to resistor $R$ variation directly affects the reference voltage. However, since both reference voltages are generated from the identical current $I_{\text{REF}}$ and capacitor $C_1$, in this case, $V_{\text{REF}}$ and $V_{\text{REF}}/32$ will be affected by the same amount of error. This will simply increase the gain error of the DAC, where the gain error does not degrade the INL and DNL. The INL and DNL of the DAC with worst case 10% $R$ variation (assuming due to process and temperature variation) showed $-0.07\text{LSB}$ and $-0.03\text{LSB}$, respectively. This justifies the reference error due to $R$ variation does not significantly degrades the performance of the proposed DAC. However, calibration scheme should be incorporated for application where DAC gain error is critical.

Switch charge injection and reference amplifier input parasitic can affect
the control pulse width and cause reference error as well. Therefore, in order to minimize the effect of charge injection and amplifier input parasitic, minimum sized CMOS transmission gate were used for the control switches, and parasitic insensitive switched capacitor configuration was employed for the reference voltage generation. In addition, the optimized value of $C_1$ and $C_2$ was chosen considering switch charge injection and amplifier input parasitic. Furthermore, to investigate the effect of switch charge injection and reference amplifier input parasitic with supply voltage variation, the DAC was simulated with $\pm 10\%$ supply voltage variation (this amount is usually considered for commercial products). However, even with $\pm 10\%$ supply voltage variation, the proposed DAC showed negligible performance degradation. This means the effect of switch charge injection and amplifier input parasitic with $\pm 10\%$ supply voltage variation can be tolerated.

5 Summary

A parasitic insensitive 10-bit C-DAC with time-mode reference generator is proposed. It is shown that the proposed DAC is insensitive to parasitic capacitance which is a major performance limiter for C-DACs. Furthermore, the time-mode reference voltage generator that replaces the conventional resistor divider can reduce the size of the reference generator and provide programmable reference voltage levels.
Acknowledgments

This work was supported by the New IT Project for global competitiveness strengthening of the advanced mobile devices and equipment of the Chungcheong Leading Industry Office of the Korean Ministry of Knowledge Economy and the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2010-0004336).