A compact-sized 10-bit two-stage DAC for AMOLED column driver ICs

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Abstract: An optimized compact-sized 10-bit DAC with one-voltage selector for AMOLED column driver ICs is proposed in this paper. By rearranging the architecture of the switch-capacitor in the proposed design, the number of decoder switches is cut in half. In addition, a compact 8-bit two-stage DAC with two-voltage selector is also presented. The simulation and experiment results show that the column drivers adopting the compact 8-bit DAC and 10-bit DAC occupy only 53.7% and 76.3% of the area required for the driver adopting the conventional 8-bit R-DAC. The measured DNL/INL is 0.44LSB/0.68LSB for the 8-bit DAC and 0.126/0.256LSB for the 10-bit DAC, respectively. Moreover, settling time within 6.43μs is achieved under 1.5kΩ-resistance and 100pF-capacitance load, hence the proposed column driver is suitable for Full-HD AMOLED displays.

Keywords: digital-to-analog converter (DAC), AMOLED displays, column driver

Classification: Electronic displays


1 Introduction
Active matrix organic light-emitting diode (AMOLED) displays have recently gained substantial attention because of their advantages over other display technologies, such as thinness, light weight, fast response and low power consumption [1,2]. Among various driving schemes for AMOLED displays, the voltage-driving method, which features fast writing time and a reduction in power consumption, is commonly adopted in commercial AMOLED displays [3]. Since the column driver outputs display data to AMOLED panel directly, its performance has a significant influence on the display quality, such as speed, accuracy and uniformity. As shown in Fig. 1, the column driver commonly includes shift register, sample latch, data latch, level shifter, DACs and output buffers. Among these components, DACs often occupy a large silicon area because each column driver contains hundreds of DACs.

Resistor DAC (R-DAC) is predominantly used in column drivers due to its uniform characteristic that stems from the commonly shared resistor-string for all channels. However, the area of the decoder in R-DAC doubles with every 1-bit increase in data [4]. This makes the R-DAC impractical for use in column driver ICs for high color depth displays. In recent years, several area-efficient two-stage DAC architectures including resistor-resistor-string DACs (RR-DACs) [5,6] and embedded DACs [7,8] have been developed for high definition display. Owing to the reduction in bit number of R-DAC, the area of two-stage DAC is efficiently decreased. However, the embedded DACs suffer greatly from matching problem.
The typical RR-DACs usually contain two internal unity-gain buffers. This will induce offset errors and increase the power consumption.

In this paper, we first present a compact 8-bit two-stage DACs containing a 5-bit two-voltage selector and a 3-bit capacitor DAC (C-DAC), which reduces the die area to some extent. And then, an optimized 10-bit DAC which consists of a voltage-selecting stage and a voltage-dividing stage is proposed to further reduce the area of DAC. Unlike the two-stage DACs which include a two-voltage selector in their first stages, the optimized 10-bit DAC only utilizes a one-voltage selector in its first stage. The proposed two-stage DAC architecture keeps the size of 10-bit data driver even smaller than that of the conventional 8-bit driver.

2 DAC Architecture

2.1 Principle of two-stage DAC with two-voltage selector

Fig. 2 schematically shows the 8-bit two-stage DAC with two-voltage selector. The 8-bit DAC can be split into 5-bit coarse section and 3-bit fine section. The 5-bit coarse section is comprised of two sets of 5-bit tree-type decoders which are arranged with 1-bit offset, and the 3-bit fine section is implemented by C-DAC. Finally, the 8-bit DAC combines these two sections in a cascade manner.

Data conversion is achieved as follows. Firstly, the two sets of 5-bit decoders in the coarse section select two adjacent voltages \( V_H \) and \( V_L \) from the global resistor according the 5-MSB and then provide them to the C-DAC as charging voltages. After that, the C-DAC realizes fine voltage division according to the 3-LSB. The detailed configuration of the C-DAC is depicted in Fig. 2(b), where C represents the unit capacitor. The basic operation of the C-DAC consists of two phases, which are pre-charge phase (\( \Phi=0 \)) and evaluation phase (\( \Phi=1 \)), respectively. As the names for the phases imply, charging and charge-sharing occur during the data conversion. As the two phases are alternated and repeated, the desired analog voltages can be obtained.

In the 8-bit two-stage DAC, there are two sets of 5-bit one-voltage selector for selecting \( V_H \) and \( V_L \). Actually, the area needed for these two 5-bit one-voltage selectors is approximately equal to that for a 6-bit one-voltage selector. Hence, for the presented 8-bit two-stage DAC, the bit number of R-DAC can be equivalent to
6. In this way, the bit number of R-DAC in the presented DAC is reduced from 8 to 6, so its area is efficiently reduced. Compared with the two-stage RR-DACs, which are reputed the most area-effective and thus the most promising candidate for column driver applications [5], this architecture features high uniformity and low static power consumption since intermediate unity-gain buffers are not required. Consequently, it is appropriate for high resolution column driver.

2.2 Optimized two-stage DAC with one-voltage selector

As the bit number of R-DAC in the two-stage DAC discussed above is decreased by 2, the number of switches required for the voltage selectors and the relevant routing lines are reduced considerably, leading to a compact chip size of the column driver. However, the aforementioned two-stage DAC as well as many other state of the art two-stage DACs contain a two-voltage selector in each DAC to choose two adjacent voltage levels from the global resistor string. These two-stage DACs are far from completely optimized because the die area required for an i-bit two-voltage selector doubles that of an i-bit one-voltage selector.

To solve the above-mentioned issues, we propose a compact-sized 10-bit two-stage DAC which merely utilizes a one-voltage selector in its first stage to further reduce the area of the column driver IC. The proposed DAC architecture is shown in Fig. 3. This DAC contains a 7-bit voltage-selecting stage and a 3-bit voltage-dividing stage. As shown in Fig. 3(a), the voltage-selecting stage is implemented by a 7-bit one-voltage selector which is controlled by the lower 7-bit \( b_{6}b_{5}b_{4}b_{3}b_{2}b_{1}b_{0} \) of the input data. The global resistor string is connected between the high reference voltage \( V_{\text{REF}} \) and ground \( V_{\text{SS}} \). The voltage-selecting stage selects one voltage named \( V_{\text{LSB}} \) from the global resistor string according to \( b_{6}b_{5}b_{4}b_{3}b_{2}b_{1}b_{0} \) and then sends it to the voltage-dividing stage. Fig. 3(b) illustrates the schematic of the voltage-dividing stage, consisting of three binary weighted capacitors, an additional unit capacitor and a set of switches that can connect the capacitors to \( V_{\text{LSB}}, V_{\text{REF}} \) or \( V_{\text{SS}} \). The switches in the voltage-dividing stage are controlled by the higher 3-bit \( b_{7}b_{6}b_{5} \) and the clock signal \( \Phi \). The timing diagram of the proposed DAC is also illustrated in Fig. 3(b). Similar to the two-stage DAC described in section 2.1, the optimized two-stage DAC also needs two phases to accomplish the
conversion, namely the pre-charge ($\Phi=0$) phase and the evaluation ($\Phi=1$) phase. As shown in Fig 3(b), $t_c$ and $t_e$ are the time for pre-charge phase and evaluation phase, and $t_h$ is the horizontal scanning time, which is determined by the display resolution and frame rate. In addition, the voltage range of clock $\Phi$ is 0-3.3V.

![Fig. 4. Operation states of the optimized DAC according to the operation phases; (a) pre-charge and (b) evaluation.](image)

The operation states of the proposed DAC when $\Phi=0$ and $\Phi=1$ are shown in Fig. 4. As shown in Fig. 4(a), during the pre-charge phase, three binary weighted capacitors are connected to the reference voltage $V_{REF}$ or $V_{SS}$ according to the higher 3-bit ($b_9-b_7$) of the input data, and the additional unit capacitor is connected to the analog voltage $V_{LSB}$, which is produced by the voltage-selecting stage. At the end of this phase, the top-plate voltages of three binary weighted capacitors reach $V_{REF}$ or $V_{SS}$. The output voltage of voltage-selecting stage can be expressed as

$$V_{LSB} = \frac{V_{REF}}{2^7} \sum_{i=0}^{6} 2^i b_i.$$  

Therefore, the charge stored in all capacitors is obtained as follows:

$$Q_{pre-charge} = C \left( V_{LSB} + b_7 V_{REF} + b_9 V_{SS} + 2 b_8 V_{REF} + 2 b_9 V_{SS} + 4 b_7 V_{REF} + 4 b_9 V_{SS} \right)$$

$$= C V_{REF} \left( \frac{1}{2^7} \sum_{i=0}^{6} 2^i b_i + b_7 + 2 b_8 + 4 b_9 \right).$$  

As shown in Fig. 4(b), when the clock signal $\Phi$ goes down to zero, all of the capacitors are disconnected from the charging voltages, and the top plates of the capacitors are connected together. As a consequence, charge sharing occurs between the capacitors, and all the voltages across the capacitors are equal to $V_{DAC}$. During the evaluation phase, the charge stored in all of the capacitors can be expressed as

$$Q_{evaluation} = 8 C V_{DAC}.$$  

Since the total charge stored in the capacitors is constant, the output voltage of the proposed DAC can be obtained from equation (2) and (3), which is shown as follows:

$$V_{DAC} = \frac{V_{REF}}{2^{10}} \sum_{i=0}^{9} 2^i b_i.$$  


Equation (4) coincides with the output expression of the standard 10-bit DAC. By this means, the 10-bit digital to analog data conversion can be realized effectively. In the proposed design, the nominal value of the unit capacitance C is set to 1pF to minimize the effects of parasitic capacitance and capacitor mismatch on conversion accuracy of the proposed DAC. Since the parasitic capacitance is much smaller than the unit capacitance, they do not contribute to conversion error significantly.

Comparing the optimized 10-bit DAC with the 8-bit DAC discussed in section 2.1 as well as many other conventional two-stage DACs, we observe that the proposed 10-bit DAC uses a one-voltage selector instead of a two-voltage selector in its first stage, so the switches required in this voltage selector is reduced nearly by half, leading to reduction in chip area. Moreover, the capacitors can be implemented using metal-insulator-metal (MIM) capacitors composed of upper metal layers. If we place them right above the voltage-selecting circuit, the chip area will be further reduced.

3 Output Buffer

In the AMOLED column driver, the DACs convert the digital display data to analog voltages, and then the output buffers drive the highly capacitive column lines to the voltage levels produced by the DACs. In this work, a rail-to-rail class B amplifier, which has large transient driving capability with little static current, is adopted, serving as the output buffer of the column driver [9].

The schematic of the output buffer is shown in Fig. 5. The input stage is made up of a rail-to-rail folded cascade differential amplifier (M1-M14), and it realizes a full-range input swing. Two comparators (M15-M18) and a class B output stage (M19-M20) are used to improve the slew rate. By introducing a zero which is induced by the load capacitor $C_L$ and the series compensation resistor $R_C$, phase compensation is performed.

![Fig. 5. Schematic of output buffer for the proposed column driver.](image)

In the rail-to-rail input stage, the aspect ratios of M7, M9, M11 and M13 are designed to be equal to that of M8, M10, M12 and M14 respectively, so that both complementary pairs of the input differential amplifier draw the same current in static state. In order to make the two comparators work properly, the following design conditions should be fulfilled:

\[
(W/L)_{15} < (W/L)_{8} < (W/L)_{17} , (W/L)_{18} < (W/L)_{14} < (W/L)_{16} .
\]  

(5)
In the AMOLEDs column driver application, the amplifier works as a unit-gain amplifier by connecting the inverting input node ($V_N$) with the output node ($V_{OUT}$). The operating principle of the output buffer is explained as follows. In the static state ($V_N=V_{OUT}$), the currents flowing through the two branches of the folded-cascade current mirror are equal. In this case, the gate voltage of M15 and M16 are equal to that of M8 and M14, respectively, so the drain currents of M8 and M14 are mirrored to M15 and M16. More specifically, as long as $(W/L)_{15}$ is smaller than $(W/L)_8$, and $(W/L)_{16}$ is larger than $(W/L)_{14}$, M16 will operate in the triode region while M15 stays in saturation region. Furthermore, the gate voltage of M18 will go almost down to $V_{SS}$, leading to the cut-off of M18. Similarly, M19 will be switched off as well. As a result, the output stage consumes no static power in static state. When a negative-going step is applied to the input node, the drain currents of M8 and M14 will be larger and smaller than the drain currents of M7 and M13 respectively, hence the drain voltages of M8 and M14 will be decreased. This will make M15 go to the triode region and M16 go to the saturation region. As a result, M19 is cut-off and M20 is switched on to discharge the output node with large current. Likewise, if a positive-going step is applied to the input node, M20 will be cut-off and M19 will be switched on to charge the output node. Consequently, this buffer draws little current during static, but has an improved driving capability during transient operation.

4 Results and Comparisons

A column driver adopting the 8-bit two-stage DAC with two-voltage selector discussed above was fabricated in 0.18-μm one-poly four-metal 1.8V/3.3V CMOS technology. Due to the limitation of available silicon area, the column driver adopting the optimized compact-sized 10-bit two-stage DACs with one-voltage selector was verified by the post-layout simulation.

Fig. 6 (a) shows the chip microphotograph of the column driver adopting 8-bit two-stage DACs with two-voltage selector and (b) layouts of single-channel driver with 8-bit two-stage DAC and 8-bit R-String DAC.
reduction by 46.4% compared with classical 8-bit R-DAC. Fig. 7 shows the transient response result of the output voltage when changing the graphic data from \((00)_{16}\) to \((\text{FF})_{16}\) with 1.5k-resistance and 100pF-capacitance load. The settling time within 0.1% tolerance of the final voltage (0V-3.287V) is 6.02μs. The glitches circled on the transient curve are caused by instability of the output buffer as well as the clock feed-through effect, both of which occur during the operation state transition of the DAC.

![Fig. 7. Transient response result of the fabricated column driver.](image)

Fig. 8 (a) and (b) show the measured DNL and INL of the fabricated 8-bit column driver. The maximum DNL and INL are 0.44LSB and 0.68LSB, respectively. The inter-chip deviation voltage output (DVO) is the key performance of the column driver which heavily affects the display quality. As shown in Fig. 8(c), the measured maximum DVO is 4.81mV, which is mainly caused by the offset of output buffers.

![Fig. 8. Measured (a) DNL, (b) INL and (c) DVO of the fabricated 8-bit column driver.](image)

To evaluate the performance of the optimized two-stage DAC with one-voltage selector proposed in this work, a 10-bit column driver is implemented and the simulation and layout results are analyzed for the linearity and area. Fig. 9 shows the single-channel layouts of drivers adopting a) the 10-bit two-stage DAC with two-voltage selector, b) the classical 8-bit R-DAC and c) the optimized 10-bit two-stage DAC with one voltage selector. All the layouts are designed using standard 0.18-μm 1P4M CMOS technology. This result shows that the optimized
10-bit DAC with one-voltage selector occupies only 60.5% and 73.4% of the areas required for a 10-bit two-stage DAC with two-voltage selector and a classical 8-bit R-DAC, respectively. Fig. 9 demonstrates that the optimized two-stage DAC proposed in this work is area-efficient.

Fig. 9. Single-channel layouts of drivers adopting (a) the 10-bit two-stage DAC with two-voltage selector, (b) the classical 8-bit R-DAC and (c) the optimized 10-bit two-stage DAC with one voltage selector.

In order to verify the proposed driving scheme, a series of 10-bit digital data varying from (000)\(_{16}\) to (3FF)\(_{16}\) are applied to the 10-bit column driver. Fig. 10 shows the transfer curve of the optimized 10-bit DAC with its output buffer. Fig. 11(a) and (b) show the measured DNL and INL of the proposed 10-bit column driver. The worst DNL and INL are measured as 0.126 LSB and 0.265 LSB, respectively. The nonlinearities are mainly caused by charge injection and clock feed-through in the second stage of the proposed DAC, where switch-capacitor model is used. These non-ideal effects can be reduced by minimizing the size of switch transistors and optimizing the value of unit capacitance.

Fig. 10 Transfer curve of the optimized 10-bit two-stage DAC.

Fig. 11. (a) DNL and (b) INL of the proposed 10-bit column driver.
Fig. 12 shows the measured output waveform with 1.5kΩ-resistance and 100pF-capacitance load, as the input data change from “000\textsubscript{16}” to “3FF\textsubscript{16}”. Settling time within 0.1% of the final voltage for a full swing (0-3.287V) is 6.43μs. For Full-HD (1920×1080) display, the horizontal scanning time is 15.43μs. Hence, the proposed column driver is suitable for Full-HD displays. Table I presents a performance summary of the presented column drivers in this work. Compared with the prior arts, the column drivers in our work are superior in die area and some other main parameters as well.

### Table I. Performance summary and comparison

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<th>Parameter</th>
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<th>[11]</th>
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<td></td>
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<td>8-bit driver</td>
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<td>0.35-μm (N/A)</td>
<td>0.35-μm (2P4M)</td>
<td>0.18-μm (1P4M)</td>
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<td>3.3/5V</td>
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<td>Setting time</td>
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<td>6.8μs 100kΩ/10.5pF</td>
<td>6.02μs 1.5kΩ/100pF</td>
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<td>0.0212mm\textsuperscript{2} (only DAC)</td>
<td>0.0332mm\textsuperscript{2}</td>
<td>0.0126mm\textsuperscript{2}</td>
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### 5 Conclusions

This paper presents a compact 8-bit two-stage DAC with two-voltage selector and an optimized area-efficient 10-bit DAC with one-voltage selector for AMOLED column driver ICs. Column drivers adopting the presented 8-bit DAC and 10-bit DAC are implemented with 0.18-μm CMOS technology and the areas are 0.0126mm\textsuperscript{2} and 0.0179mm\textsuperscript{2}, which are much smaller than the column driver with 8-bit R-DAC. The measured DNL/INL is 0.44LSB/0.68LSB for the 8-bit DAC and 0.126/0.256LSB for the 10-bit DAC, respectively. Settling time within 6.43μs is achieved under 1.5kΩ-resistance and 100pF-capacitance load, hence the proposed column driver is suitable for Full-HD AMOLED displays.

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