A Reliability Improved Synchronous Boost Converter with Spike Suppression circuit

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Abstract: A reliability improved synchronous boost converter with spike suppression circuit is proposed in this paper. Compared with the traditional boost converter, a novel control circuit is designed to suppress the voltage spike at node SW during the dead time. In addition, the two main power switches could be avoided to operate in ON state during the transient process. Hence, both the reliability and the efficiency are improved. The converters with/without spike suppression circuit are designed and implemented in a 0.5μm standard CMOS processes. The experimental results show that the voltage spike at node SW is reduced 43% when the load current is 0.5A, and the efficiency is improved at light load.

Keywords: Reliability, Synchronous Boost Converter, Spike Suppression

Classification: Integrated circuits

References

1 Introduction

With increasing demand for power management in consumer and portable applications, switching converters, which supply highly integrated systems over a chip, have attracted more attention due to the advantage of high efficiency and output capability in the field of power electronics.

The efficiency of a switching converter is mainly restricted by conduction loss, switching loss, and quiescent current loss. The boost converter, which is capable of producing a dc output voltage magnitude larger than that of dc input, is widely used in power supply systems. In asynchronous boost converter, the conduction loss is mainly caused by the forward voltage drop of the diode. Besides, the inductor current which coincides with the dc input current in boost converter is greater than the load current. Therefore, diode conduction loss is easily the largest source of power losses. To reduce the forward voltage drop, Schottky diodes having reduced junction potential can be employed; nonetheless, the efficiency is restricted in low-voltage power supplies that conduct large current applications.

To achieve high efficiency in low voltage applications, the concept of a synchronous rectifier is widely utilized in both isolated and non-isolated DC-DC converter [1], the reverse-conducting capability of the metal-oxide semiconductor field-effect transistor (MOSFET) allows it to be used where a diode would normally be required. The conduction loss of a MOSFET with on-resistance $R_{ON}$ and operates under the RMS current of $I_{RMS}$ is $I_{RMS}^2R_{ON}$. The $R_{ON}$ can be decreased by increasing the size of the MOSFET. So the conduction loss can be reduced as desired with the cost of larger die size. However, along with the introduction of the extra power switch in synchronous converter, the timing of the control signal becomes complicated. And the turn on/off process of the synchronous rectifiers primarily must be carefully designed because of two factors: Firstly, because the MOSFETs can not block reverse current automatically like diodes, so the properly turn-off signal should be applied to the synchronous power switch, otherwise, a reverse current flows from the output terminal to the input power supply, which causes large efficiency loss, especially in discontinuous mode (DCM). Secondly, the main power MOSFET and the synchronous switch should be avoided to operate in ON state simultaneously because that the shoot-through current between two power switches will ruin the converter. So, a dead-time [2,3] is inserted to the gate control signals. In order to improve the efficiency, various literatures are reported to optimize the dead-time [4-10]. In [6], the dead time of the power transistors can be dynamically optimized under any load condition. In [8], a senseless dead-time controller exploits a complex digital algorithm to search the optimal dead-time through a long period. The efficiency can thus be improved. However, during the dead time, both the power transistors are operated in OFF state, the voltage spike occurs at node SW due to the di/dt property of the inductor, therefore the voltage stress imposed on the power switch is increased. The efficiency and reliability are degraded.

Few literature are reported to suppress the overshoot during the dead time in synchronous converters. In this paper, a novel switching node spike voltage
suppression circuit is proposed, which improves the reliability of the synchronous boost converter. Compared with the traditional boost converter, a novel control logic circuit is proposed to reduce the voltage stresses imposed on the power switch during the dead time. And the reliability and efficiency are improved simultaneously.

This paper is organized as follows: The traditional synchronous boost converter is described in section 2. The presented reliability improved synchronous boost converter with a novel control circuit is depicted in section 3. The test results and discussions are shown in section 4. Finally the conclusion of this paper is given in section 5.

2 Synchronous Boost Converter

A traditional synchronous boost converter is shown in Fig. 1, in which power transistors M1 and M2 are main power switches. M3 and M4 constitute the body selector circuit. When the control signal PG is low, the transistor M2 turns on, if the input voltage VIN is larger than the output voltage, the switch M3 turns on and the body of the transistor M2 is connected to the input voltage VIN, otherwise, it is connected to the output voltage VOUT to guarantee the correct timing when the transistor M2 turns on.

During the interval t2 < t < t3, both the gate control signals are high, the power switch M1 turns on and M2 turns off; during the period t > t4, both the gate control signals are low, the power switch M1 turns off and M2 turns on, respectively. To improve the efficiency and reliability, the M1 and M2 are avoided to turn on simultaneously, therefore, an appropriate dead time (t1 < t < t2, t3 < t < t4) is
designed. During the period of $t_1 < t < t_2$, $M_2$ turns off before the $M_1$ turns on. During the interval of $t_3 < t < t_4$, the gate control signal of $M_1$ goes to low and the gate signal of $M_2$ still keeps high, the current of the inductor reaches the maximum value. In order to keep the current of the inductor continuous, the body diode of $M_2$ and $M_4$ are forced to turn on, and the voltage at node SW can be expressed as:

$$V_{SW} = V_{OUT} + V_{D2} + V_{DS,M4} + L_{par} \frac{di(t)}{dt}$$  \hspace{1cm} (1)

Where $i(t)$ is the current of the inductor, $L_{par}$ is the parasitic inductor of the bounding wire, $V_{D2}$ is the forward voltage of body diode of $M_2$, $V_{DS,M4}$ is the voltage drop of the transistor $M_4$, $V_{SW}$ is the switching node voltage, $V_{OUT}$ is the output voltage. It can be shown from (1), during the dead time, both of the power switches turn off, this increases the voltage stresses applied to transistor $M_2$. It is worthy emphasizing that voltage drop of $M_4$ is larger than the power switch $M_1$ and $M_2$ due to the large on-state resistance. In addition, for a larger load current, larger $V_{DS,M4}$ and $di(t)/dt$ is. The worst-case occurs during the subinterval $t_3 < t < t_4$ since the current is larger than that of subinterval $t_1 < t < t_2$ as shown in Fig. 2. Therefore, the reliability and efficiency of the converter are both affected.

3 The Proposed Boost Converter

As stated in the previous section, during the dead time, both the power switch $M_1$ and $M_2$ are operated in OFF state, the voltage spike occurs at node SW. To reduce the stresses of the power switch, a reliability improved synchronous boost converter with spike suppression circuit is shown in Fig.3. Compared with the traditional boost converter, an extra control circuit is designed to suppress the voltage spike at node SW during the dead time. The timings of the main control signals are shown in Fig. 4.
During the dead time $t_3 < t < t_4$, the signal $NG$ turns high to low and $PG1$ still keeps high, the voltage at node SW starts to increase. A negative pulse signal $VA$ is produced at node A simultaneously. The pulse width of the signal is produced by the delay timer ($TD$) and the transmission delay time of the inverter INV. Once the voltage at node SW increased to higher than the threshold voltage of $MS3$ ($VTH$), the transistor $MS3$ turns on, then the gate signal ($PG1$) of the synchronous power switch is pulled down by $MS3$, which turns on $M2$. It is noted that the negative pulse signal ($VA$) should keeps low until $M2$ turns on totally. In addition, the synchronous gate signal ($PG1$) is driven by the signal SW, the SW node voltage keeps low until the MOSFET $M1$ turns off completely. Therefore the two power switches $M1$ and $M2$ are impossible to operate in ON state at the same time. The voltage at node SW during the rising edge dead time $t_3 < t < t_4$ can be expressed as:

$$V_{SW} = V_{out} + V_{DS,M2} + L_{par} \frac{di}{dt}$$

(2)

Where $V_{DS,M2}$ is the voltage drop of the synchronous PMOS $M2$. Compared to (1), the $V_{SW}$ difference between the proposed boost converter and the conventional is derived as:

$$V_{SW,DIFF} = \left[ V_{OUT} + V_{D2} + V_{DS,M4} + L_{par} \frac{di(t)}{dt} \right] - \left[ V_{out} + V_{DS,M2} + L_{par} \frac{di(t)}{dt} \right]$$

$$= V_{D2} + V_{DS,M4} - V_{DS,M2}$$

(3)

From equation (3), $V_{SW,DIFF}$ is determined by $V_{D2}$, $V_{DS,M2}$ and $V_{DS,M4}$, where $M2$ is the main synchronous power switch, $M4$ is the body selector switch, $V_{DS,M2}$ is much smaller than $V_{DS,M4}$ under the same conduction current condition. Furthermore, $V_{D2}$ is the forward voltage of the synchronous power MOSFET body diode, in most integrated circuit processes, this value is about 0.7V. In conclusion, the proposed circuit can obviously reduce the overshoot voltage at node SW.

The relations between the power dissipation ($P_{DEADTIME}$) and the SW spike voltage during the dead time can be shown as [11]:

![Fig. 4. Timing of the proposed boost converter.](image-url)
\[ P_{\text{DEADTIME}} \propto f_{SW} \cdot \frac{C_{SW,\text{PAR}} V_{SW}^2}{2} \quad (4) \]

Where the \( C_{SW,\text{PAR}} \) is the total parasitic capacitance at node SW, \( f_{SW} \) is the switching frequency of boost converter. In (4), the power dissipation during the switching transition is proportional to the square of \( V_{SW} \). In addition, the power consumption is reduced significantly with the decrease of the \( V_{SW} \).

### 4 Experimental Results

To verify the validity of the design strategy, two synchronous boost converters with/without spike suppression circuit are designed and fabricated in a 0.5 μm standard CMOS process for comparison. The main parameters are given by \( V_{IN}=3.3 \text{V}, V_{OUT}=5.1 \text{V}, L=4.7 \mu \text{H}, C_{OUT}=10 \mu \text{F} \). The micrograph of the synchronous boost converter with the proposed spike suppression circuit is shown in Fig. 5, and the spike suppression circuit module only occupies relatively small space.

![Fig. 5. Timing of the proposed boost converter.](image)

When the load current is 0.5A, the inductor current (\( I_{CON} \)) and the voltage at node SW (\( V_{SW} \)) waveforms of the boost converter with/without spike suppression circuit are shown in Fig. 6 and Fig. 7, respectively. It is clearly shown that the voltage spike at the node SW are about 1.65 \text{V} and 2.9\text{V}, the spike at node SW is reduced about 43% due to the adoption of spike suppression circuit. In addition, the voltage spike at \( t= t_2 \) is much smaller than that of \( t= t_3 \) as stated in the previously section.

![Fig. 6. SW voltage with the proposed circuit.](image)
The boost converters with/without spike suppression circuit under different load conditions are also measured and the results are shown in Fig. 8. It is clearly shown that the peak value at SW node is increased slowly while the conventional one rises quickly with the increase of load current. Because of the spike suppression circuit, the peak voltage of SW node is less than 7V when the load current is less or equal to 1.0A. In most 5V standard CMOS processes, the breakdown voltage of the MOSFETs is about 9V, therefore, the reliability of the boost converter is improved.

![Fig. 8. \( V_{SW} \) increase VS \( I_{LOAD} \)](image)

Fig. 8. \( V_{SW} \) increase VS \( I_{LOAD} \).

![Fig. 9. Boost converter efficiency VS \( I_{LOAD} \)](image)

Fig. 9. Boost converter efficiency VS \( I_{LOAD} \).

Fig. 9 shows that the efficiency of the boost converter with/without the proposed
circuit. The efficiency is improved obviously under light load; otherwise, when the load increases, the switching power dissipation can almost be neglected, so the efficiency improvement is not obvious.

5 Conclusion
A reliability improved boost converter with spike suppression circuit is presented in this paper. Compared to the traditional boost converter, a novel control circuit is designed to suppress the voltage spike at node SW. The reliability and efficiency are both improved. The converter is designed and implemented in a 0.5μm 5V standard CMOS process. The test results show that the proposed circuit can reduce the SW node stress and improve the efficiency at light load application.

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