A single-poly EEPROM with low leakage charge pump and peripheral circuits for passive RFID tag in a standard CMOS technology

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Abstract: A complete single-poly 2k-bit EEPROM solution including memory cells and peripheral circuits is presented and embedded into a passive RFID tag using a 0.18-µm standard CMOS technology. A charge pump with a Diode-C all-pass network and peripheral circuits without static current are proposed to reduce power consumption. A three-transistor memory cell is adopted for CMOS-compatibility, low operation voltage, and low complexity of drivers. The proposed EEPROM occupies an active area of 0.21 mm². The leakage current during read operation is 36 nA from 1-V supply, while the static current during write operation is 1.3 µA from 1.8-V supply.

Keywords: charge pump, EEPROM, low leakage, peripheral circuits, single-poly, UHF RFID tag

Classification: Integrated circuits

References


1 Introduction

The Ultra-High-Frequency (UHF) Radio Frequency Identification (RFID) applications increase rapidly in recent years. Different from an active tag, a passive tag could harvest energy from radio frequency signal and is not limited by battery life, so that it can be applied in supply chain, access control, asset management system, etc. However, the passive tag still faces two issues: the cost of a chip and the sensitivity level which is limited by power consumption.

As one of the key blocks in a RFID tag, the non-volatile memory (NVM) that includes memory cell array and peripheral circuits consumes a significant part of total chip area and power consumption. Although some new type NVMs, such as ferroelectric RAM (FeRAM) and resistive RAM (RRAM), have advantages on chip area and power consumption [1, 2], it requires a special process which would increase cost. Electrically erasable programmable read-only memory (EEPROM) is most widely adopted for its CMOS compatibility and reliability [3-4]. A conventional EEPROM cell is implemented by a floating gate in a double polysilicon (2P) technology which requires many addition masks and high operation voltage (15~20V), increasing the cost and power dissipation. Several single-polysilicon EEPROM cells have been proposed in recent years to reduce process cost [5-9]. A two transistors (2-T) cell could reduce chip area, but it needs much more complex peripheral circuits [10].

This paper presents a low power single-poly EEPROM solution including memory cells and circuits in a standard CMOS technology. A charge pump with a Diode-C all-pass network is utilized to reduce static current. The peripheral circuits for memory array without static current are employed for low power consumption. A
A power configuration scheme is proposed to isolate all drivers from high voltage to reduce leakage current when it is not during write operation. The memory array also adopts a three-transistor (3-T) cell with selection device to reduce operation voltage and complexity of peripheral circuits which could decrease power dissipation further. The proposed EEPROM has been fabricated in a standard 0.18-μm CMOS technology and embedded into a passive RFID tag.

2 Architecture of the proposed EEPROM

The architecture of the proposed 2k-bit EEPROM is shown in Fig. 1, composed of a charge pump and two 1k-bit pages. Each page consists of a 32x32 single-poly EEPROM cell array with peripheral circuits, including drivers and readout circuits, a power configuration module to generate the power supplies for row and column drivers and a logic module to control the operation. The 1k-page can be turned-off to minimize the leakage current if unselected. The charge pump, which is only activated during write operation, could generate two boosted voltages from a voltage of rectifier (VRECT). The other circuits are supplied by a 1-V voltage from regulator. A reference clock of 640 kHz and a reference voltage of 0.65V is also provided by analog/RF frontend of a passive tag.

3 Single-poly EEPROM in standard CMOS technology

A single-poly EEPROM cell which is similar to [5] is adopted in this work, as shown in Fig. 2. Each cell consists of four devices, including control capacitor C1, tunneling capacitor C2, read transistor M1 and selection transistor M2. The
capacitors are both n-type accumulate mode varactors, located in an n-well, respectively. The read and selection devices are both p-channel transistors.

Because the n-well to substrate junction breakdown voltage of this 0.18-μm technology is about 11 V, a reliable high voltage (VDDH) for program and erase operation should be less than 10V. Thus, a larger C1 is required for high coupling factor so that the write voltage could be reduced to 9.5 V in this work. The conditions for each operation are also listed in Fig. 2.

The memory array consists of 32 columns by 32 rows, which is shown in Fig. 3. Each two columns share one readout circuit. A dummy row is adopted as reference for read operation.

During read operation, all control-gates (CGs) and tuning-gates (TGs) are set to zero. The word-lines (WLs) of all unselected rows are set to high level. Due to the threshold voltage variation after programing or erasing, the current of memory cell would change from more than 10 μA to less than 1 nA, which can be compared with the dummy cell by a readout circuit.

During program and erase operation, a protect voltage (VDDM), which is half of high voltage (VDDH), is applied for the unselected cells. All word-lines are set to zero. The voltage configurations of CG and TG are listed in Fig. 3.

4 Charge pump with Diode-C all-pass network

The current load of charge pump includes not only level shifters and drivers, but also the voltage divider of its feedback loop. A resistor voltage divider (Fig. 4(a)) requires much too large resistance (>100MΩ) to achieve a low static current, which occupies huge chip area. A capacitor voltage divider (Fig. 4(b)) does not consume any current, but the parasitic capacitance influences accuracy of divider ratio. In addition, the floating node between capacitors could be easily dropped by electric charge from ion injection during manufacture or leakage current from poly-gate.
This work adopts a Diode-C all-pass network which is shown in Fig. 4(c), consisting of 15 stages. Each stage has a forward biased diode and a capacitor, which are both implemented by a p-channel transistor and located in the same n-well. Though reverse biased diode consumes much lower current, but the leakage of substrate would influence the divider ratio seriously. As shown in Fig. 5, the network consumes a leakage current of less than 1 nA at room temperature, which is two orders of magnitude larger than substrate leakage. Besides, the leakage current would increase with temperature to about 3.5 nA at 85°C. However, the divider could only track the voltage at a very slow frequency due to the ultra-low current, which would increase the group delay of feedback network and lead to a larger ripple of the output voltage. A capacitor in parallel with each diode could achieve an all-pass network to provide a large bandwidth. The AC magnitude of feedback network with and without parallel capacitor is shown in Fig. 4 (d), which indicates that the AC magnitude of network with capacitor almost keeps constant in the whole frequency range.

The core of charge pump is based on a 10-stage Dickson architecture which is
shown in Fig. 6. The voltage of VDDM is generated by a source follower whose bias voltage also comes from voltage divider. The comparator and clock drivers are also supplied by rectifier to improve the efficiency, rather than 1-V voltage.

5 Peripheral circuits without static current

Besides a shared charge pump, the peripheral circuits of each page include power configuration, drivers and readout circuits. The most challenge in a passive tag is the current limitation from power supply, which requires to eliminate static current, especially from high voltage.

5.1 Inverters-latch based drivers

A driver for TG or CG should provide four voltage levels, which leads to an extremely complicated structure. However, only two voltage levels are required at a specific operation. Therefore, an inverters-latch based driver with a power configuration in Fig. 7 could be employed to simplify logics and eliminate static current.

![Inverters-latch based drivers and voltage configuration](image)

The inverters are composed of thick oxide transistors and served as a latch. The pull-down transistors are used to configure the output level of the latch. Each write operation is divided into two steps. A configuration step is to set the output of latch as high level or low level. Then, in the following operation step, the corresponding high voltages for program or erase, which is listed in Fig. 7, will be applied to the latch, while the configuration transistors are turned off by two AND gates. Thus, the drivers do not consume any static current from high supply voltages.

The configuration devices compose of two stacked transistors. A thick oxide native transistor could work in a low supply voltage of VDD, but faces a problem of leakage current in cutoff region, which can be reduced by a stacked thin oxide normal transistor. A pair of thick oxide native transistors are employed to protect configuration devices from high voltages.
5.2 Power configuration module

The supply voltages and bias voltages for row and column drivers are generated by a power configuration module, composing of several level shifters, as shown in Fig. 8. There are four types of level shifters to generate differential voltages. Considering that the outputs (VDDH and VDDM) are high impedance when charge pump is disable, the level shifters of bias voltage configuration should provide a 1-V output for the following circuits. The level shifters for row and column supplies could work properly with a 1-V supply voltage or high supply voltages.

Fig. 8. (a) power configuration module and level shifter of (b) VDDM/VDD, (c) VDDH/VDD, (d) VDDM/GND and (e) VDDH/VM

All level shifters do not consume static current in this work. Thus, the leakage current has a significant portion of power consumption, especially the leakage from high supply voltage (VDDH). The leakage mainly comes from sub-threshold leakage of lever shifters and drivers, and n-well to substrate junctions. With a supply voltage of 10 V, the leakage current of a selected 1-K page including lever shifters, drivers and cells is shown in Fig. 9. Besides, when a page is unselected, the power configuration module only applies 1-V voltage to the following drivers and reduce the leakage from VDDH to less than 1 nA.

Fig. 9. Simulated leakage current of a 1-K page from a 10-V supply
5.3 R-S latch-based readout circuits
The readout circuit could benefit from the 3-T cell and is isolated from high voltage which makes it possible to simplify the circuits and reduce power consumption. An R-S latch-based sense comparator without static current is presented in Fig. 10. Because two columns share one readout circuit, a multiplexer (BL_MUX) is adopted to select one bit-line from two.

A read operation includes three states: pre-set, sensing and latch. When signal EN_RW is low, the inputs of R-S latch are forced to low and the outputs are both high level. When EN_RW goes high, the currents of selected cell and dummy cell will charge $V_A$ and $V_B$, respectively. Because of the positive feedback, either $V_X$ or $V_Y$ would increase to high level and keep in a latch state until EN_RW falls down. There is no static current during pre-set and latch state.

6 Experiment results
A passive RFID tag with the proposed single-poly EEROM array with peripheral circuits has been fabricated in a standard 0.18 $\mu$m CMOS 1P6M technology. The 2k-bit EEPROM only takes up three metal layers and occupies an active area of 0.21 mm$^2$, including an area of 160 $\mu$m x 90 $\mu$m for charge pump. Fig. 11 shows the micrograph of the passive UHF RFID tag.

The memory cells have been measured by probe station on wafer. The threshold voltages by various operation conditions are shown in Fig. 12, which indicate that 9.5-V voltage with 1-ms operation time could bring about a voltage window greater than 1.8 V and is utilized as rated condition.
Fig. 13(a) shows the reliability characteristics of endurance of three cells. The voltage windows are degenerated by 200 mV after 10-k cycles. The retention characteristics of cell before and after stress are measured at 85 °C [11] and shown in Fig. 13(b). The threshold voltage window would be degraded by 0.5 V.

The average dynamic power consumption of byte-wise read operation is 2.7 μW with a 320 kHz period. Besides, the measured leakage current from 1-V supply is 36 nA in room temperature.

Fig. 14 shows the drive capacity of charge pump with different supply voltages. On account of no static current, the charge pump only consumes 1.3 μA current to keep the output voltage at an average voltage of 9.77 V when supply voltage is 1.8 V. The current consumption increase to 3.1 μA while supply voltage is 3.0 V.
In practice, due to the limited drive capacity of rectifier, the supply of charge pump is not a stable voltage. Fig. 15 shows the time response of the charge pump with a supply from rectifier. With an -14-dBm input power at 840-MHz, the rectifier could provide a 2.1-V supply voltage. However, due to the power consumption during start-up of charge pump, the voltage would drop to 1.6 V and then goes up when charge pump reaches stable voltage.

![Fig. 15. Time response of charge pump with a supply from rectifier](image)

### 7 Conclusion

A single-poly 2k-bit EEPROM solution including memory cells and peripheral circuits is presented and embedded into a passive RFID tag using a 0.18-µm standard CMOS technology. A charge pump with a Diode-C all-pass network and peripheral circuits without static current are proposed to reduce power consumption. A power configuration scheme is proposed to isolate all drivers from high voltage to reduce leakage current when it is not during write operation. A three-transistor memory cell with a selection device is adopted for CMOS-compatibility, low operation voltage, and low complexity of drivers. The proposed EERPOM occupies an active area of 0.21 mm². During read operation, the measured leakage current is 36 nA from 1-V supply and dynamic power consumption is 2.7 µW. The static current during write operation is 1.3 µA from 1.8-V supply and increases to 3.1 µA while rectifier voltage is 3.0 V.

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