A 6-Bit 38GHz SiGe BiCMOS phase shifter for 5G phased array communications

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Abstract: This paper presents a 6-bit 38GHz vector-summing phase shifter developed for 5G phased array communications. A linear gain adjustment VGA with modified gain control method is presented and is used in phase shifter for vectors weighting. Combined with a degenerated-Q quadrature all-pass filter (QAF) for accurate I/Q generation, high phase resolution is achieved with easy control and compact size. Fabricated in 0.13um SiGe BiCMOS process, the phase shifter has a measured average insertion loss of 5.7dB at 38GHz center frequency, with -3 dB bandwidth of 12 GHz. The RMS phase and gain errors are less than 1.7° and 1.5dB respectively across 20-45GHz frequency range over 64 phase states. The chip has a compact core size of 373um×311um and it consumes 11.2mA from 3V supply.

Keywords: phase shifter, phased array, millimeter wave, BiCMOS, Ka-band, 5G communications

Classification: Integrated circuits

References


1 Introduction

The mobile communication industry has experienced tremendous growth in recent years, and the next generation mobile communication system, 5G, will be commercialized in 2020. 5G is demanded to provide larger capacity, higher data rates and lower latency. With frequency bands below 6 GHz overcrowded, the use of mm-wave for 5G is being actively pursued in order to provide more spectrum resources for mobile communication [1, 2, 3]. 28GHz and 38GHz in Ka-band are two prime candidates considered for 5G. For full use of mm-wave in mobile communication, phased arrays are expected to compensate for high propagation attenuation, provide non-line-of-sight transmission and spatial multiplexing. The phase shifter is one of the most critical building blocks in phased array front end. Switched-type passive phase shifter [4, 5, 6, 7] has high linearity, but suffers from high insertion loss in silicon process and consumes large chip area to achieve high phase resolution. Active phase shifter [8, 9, 10, 11, 12, 13] applying vector summing method provides high phase resolution and compact size. These features make it suitable for both handset-side which demands small form factor and base-station-side that applies large-scale phased array for mm-wave massive MIMO. However, active phase shifter usually needs complex control circuits or
calibration to achieve high phase resolution or accuracy. In this work, a linear gain adjustment VGA with modified gain control method is presented and is used in phase shifter for vectors weighting. It also provides constant load impedance to previous stage. These features simplify the control of the phase shifter. Combined with highly accurate QAF I/Q generator, the presented phase shifter centered at 38GHz 5G frequency band achieves high phase resolution with easy control.

2 Topology of the vector summing phase shifter

Fig. 1 shows the block diagram of the active phase shifter in this work. Vector summing method is applied as this method offers high phase resolution easily in a smaller chip area compared to the passive phase shifter topologies. In this design, the input single-ended signal is firstly converted into differential signal via a transformer balun. Then the differential signal is fed to a quadrature signal generator which yields the in-phase and quadrature vectors. Finally, two VGAs scale the I/Q vectors independently and sum them in the current domain to synthesize the target phase. A buffer is added for measurement and output balun is used for differential to single-ended conversion and output impedance matching. The I/Q generator and VGAs for vectors weighting are the two critical blocks.

3 Differential quadrature signal generator design

Fig. 2. (a). Degenerated-Q QAF for differential I/Q generation; (b) Single-ended model of QAF; (C) Phasor diagram at resonance.
The I/Q generation block is a critical part in a vector summing phase shifter, as its performance has a big effect on the phase interpolation quality. Its key performance specs include quadrature phase and amplitude accuracies, signal loss and bandwidth. In RF frequency bands, RC-CR pair and its poly-phase filter are commonly used to generate the quadrature signals. However, they suffer from inherent signal loss and sensitivity to process variations. In addition, differential quadrature vectors are needed to synthesize all four quadrant phases.

In this work, a degenerated Q value quadrature all-pass filter [11] is employed to generate the differential in-phase and quadrature vectors as shown in Fig.2 (a). It yields signals with tight amplitude and phase balance over wide bandwidths with a low return loss at the input port. Fig.2 (b) and (c) show the single-ended model of QAF and phasor diagram respectively. Parasitic loading capacitance causes I/Q errors and these errors are large at millimeter-wave frequency. The resistors Rs are connected in series with the inductors and capacitors to decrease Q of the branch, thus minimize the capacitive loading effect from the following VGAs.

The phase and amplitude performances of input balun are also important. The center tap of the input balun’s secondary turn is grounded for low common mode impedance to provide a balanced differential signal. Careful layout design and EM simulation are done to make sure the quadrature accuracy. Shown in Fig.3, the EM simulation results including the input balun and VGA’s loading effects, show I/Q phase and amplitude errors less than 3° and 1 dB respectively over 20-45GHz frequency range. The insertion loss is about 6dB at 38GHz as shown in Fig.3 (b).

**Fig. 3.** (a) I/Q generator EM 3D model; (b) Simulated I/Q generator insertion loss; (c) Simulated I/Q amplitude error; (d) Simulated I/Q phase error.
4 Variable gain amplifier with modified gain control method

The architecture of the vector modulator is shown in Fig.4. The differential I/Q output signals from quadrature generation network are fed into two variable gain amplifiers. The weighted currents from I/Q paths are combined at the output inductive load.

![Diagram of vector modulator](image)

**Fig. 4.** Vector modulator using linear gain adjustment VGA.

Referring to the I path VGA in Fig.4, the core of VGA is a differential current-steering design. Although similar topology is used in the active phase shifters in [8, 9], the differentiation is the gain control scheme. In [8], MOS implementation of current-steering VGA is used and the variable gain is realized by changing the tail current of quad transistors (the same location as Q1,...,Q3). The differential I/Q signals from quadrature generation network are fed at the gate of the quad transistors. Thus, input impedance looking into the gate of the quad transistors changes with tail current. This causes a variable loading impedance to the I/Q generator, which will affect the I/Q performance. Meanwhile, a linear gain versus input control cannot be achieved in that design. So, to synthesize a high resolution phase shifter, a complex control circuit and logic are needed. In [9], HBT implementation of current-steering VGA is applied and the gain adjustment of VGA is realized by feeding an inverse-tanh-function voltage on the base of the quad transistors. The measured gain vs control voltage is also not linear.

In this work, linear gain adjustment is achieved with a modified gain-control method. This method makes use of the transconductance characteristic of HBT in BiCMOS process as described below. The transconductance of HBT is proportional to the collector current as in equation (1). Hence, the operating currents \((I_{1},...,I_{4})\) of the quad HBTs (Q1,...,Q4) determines transconductance ratio \((g_{m1}/g_{m2})\), thus the signal current steering ratio \((i_{1}/i_{2})\), as in equation (2). Differential output currents \((I_{P,DAC}, I_{N,DAC})\) of a current-steering DAC are fed into two diode connected HBTs (Q7, Q8). The differential voltage developed on the two diode connected HBTs are used to bias VGA quad HBTs. The bottom diode-connected HBT (Q8) is used to bias the input differential pair (Q5, Q6) of
VGA. Thus, the operating currents of quad transistors and input differential pair are determined through mirroring approach by driving a diode-connected half portion of the VGA.

\[ g_m = \frac{qI_c}{kT} \]  

(1)

\[ \frac{i_1}{i_2} = \frac{g_{m1}}{g_{m2}} = \frac{I_{c1}}{I_{c2}} \]  

(2)

Equations (3)-(5) derive the output current of VGA.

\[ i_1 = -i_4 = \frac{g_{m1}}{g_{m1} + g_{m2}} i_{in} = \frac{I_{c1}}{I_{c1} + I_{c2}} i_{in} \]  

(3)

\[ i_2 = -i_3 = \frac{g_{m2}}{g_{m1} + g_{m2}} i_{in} = \frac{I_{c2}}{I_{c1} + I_{c2}} i_{in} \]  

(4)

\[ i_{op} = -i_{on} = i_1 + i_2 = \frac{I_{c1} - I_{c2}}{I_{c1} + I_{c2}} i_{in} \]

\[ = \frac{M \cdot (I_{P,DAC} - I_{N,DAC})}{M \cdot (I_{P,DAC} + I_{N,DAC})} i_{in} = \frac{I_{out,DAC}}{I_{P,DAC} + I_{N,DAC}} i_{in} \]  

(5)

In equation (5), M is the size ratio of the HBTs (Q1,...,Q4) to HBTs (Q7, Q8) or HBTs (Q5, Q6) to HBT (Q9). Because \( I_{P,DAC} + I_{N,DAC} = I_{DAC} \) is constant, the bias of the input differential pair of VGA is ideally fixed to provide constant loading impedance to the I/Q generation network. This constant impedance feature is beneficial as I/Q performance will not be affected when adjusting VGA’s gain to shift phase. Here, set differential output current of DAC \( I_{out,DAC} = a \cdot N \), where \( N \) is the corresponding decimal value of the DAC’s binary input. The transconductance gain \( (G_m) \) of VGA is expressed as below:

\[ G_m = \frac{I_{out,DAC}}{I_{P,DAC} + I_{N,DAC}} g_{m,in} = \frac{\alpha \cdot N}{I_{DAC}} g_{m,in}, \]  

(6)

where \( g_{m,in} \) is the transconductance of the input pair of VGA. Thus, the gain of VGA can be linearly set by DAC input value. In this work, a 7bit DAC is designed with \( N \) ranges from -63 to 63.

Fig. 5 (a) shows the simulated VGA gain vs DAC input value. Linear gain with DAC input value is achieved which verifies the above analysis. The gain of MOS implementation of the same topology is also included for comparison. The linear gain is no longer effective, because the transconductance is proportional to the square root of operating current in MOS FETs. It should be emphasized that this linear gain adjust method is only effective in BJT or HBT implementations. In Fig. 5 (b), the simulated input impedance of VGA vs DAC input value is plotted, showing nearly constant impedance.
The presented VGA is used in the vector modulator shown in Fig. 4 to synthesize the target phase. Thanks to the feature of linear gain adjustment of VGA, the output phase can be easily controlled and set by the following equation:

\[ \theta = \tan^{-1} \frac{N_Q}{N_I}, \]  

where \( \theta \) is the target phase, \( N_I \) and \( N_Q \) are DAC’s input values of I path and Q path, respectively. Fig. 6 (a) shows the EM 3D model of vector modulator with two VGAs. Careful layout and EM design are needed to be done. Combining this linear gain adjustment VGA with the highly accurate QAF I/Q generator presented in section 3, a vector-summing phase shifter shown in Fig. 1 is designed at 38GHz 5G frequency band. Fig. 6 (b) shows the simulated real and imaginary parts of S21 of the whole phase shifter at 38GHz. Here, only 32x32 matrix of S21 is shown for clear display. A uniform constellation is achieved.
5 BiCMOS prototype and measurement results

The phase shifter was fabricated in GlobalFoundries 8HP 0.13um SiGe BiCMOS process. Fig. 7 shows the chip micrograph with a core size of 373um×311um. The phase shifter consumes 11.2mA from 3V supply, excluding the buffer. The on-chip S-parameters characterizations were conducted by the vector network analyzer, after performing the short-open-load-through (SOLT) calibration. Fig. 8 (a) and (b) show the measured 6-bit phase and gain responses, respectively. The phase covers 360° and the average insertion loss is 5.7dB at 38GHz center frequency. The phase shifting has a wide bandwidth due to the used degenerated-Q QAF and linear gain adjustment VGA. The amplitude response (S21) -3dB bandwidth is from 31GHz to 43GHz, limited by the LC load.

![Chip micrograph of the phase shifter.](image.png)

**Fig. 7.** Chip micrograph of the phase shifter.

![6-bit phase response](image.png)

**Fig. 8 (a).** Measured 6-bit phase response of the phase shifter.

![6-bit gain response](image.png)

**Fig. 8 (b).** Measured 6-bit gain response of the phase shifter.
Fig. 9 (a) and (b) show the measured input and output return losses with simulated results respectively. The EM simulation results show good agreements with the measured results.

The root-mean-square (RMS) phase and gain errors of the phase shifter are characterized according to

\[
\text{RMS phase error} = \sqrt{\frac{1}{N-1} \times \sum_{i=2}^{N} |\theta_{\Delta i}|^2} \quad \text{(deg.)} \quad (7)
\]

\[
\text{RMS gain error} = \sqrt{\frac{1}{N} \times \sum_{i=1}^{N} |A_{\Delta i}|^2} \quad \text{(dB)} \quad (8)
\]

where \(N\) is number of phase shifting states, \(\theta_{\Delta i}\) is the phase error corresponding to the \(i\)th ideal phase value, and \(A_{\Delta i}\) is the value of the difference between the \(i\)th insertion gain and the average insertion gain in all phase-states in dB-scale [7]. The RMS phase error is less than 1.7° over 20-45GHz as shown in Fig. 10 (a), achieving 6-bit phase resolution. Fig. 10 (b) shows the RMS gain error of less than 1.5dB, over 20-45GHz.

Fig. 9. (a) Measured input return loss over 64 phase states; (b) Measured output return loss over 64 phase states.

Fig. 10. (a) Measured RMS phase error over 64 phase states; (b) Measured RMS gain error over 64 phase states.
Measured IP1dB vs phase states at 38GHz is shown in Fig. 11 (a). IP1dB varies in the range of -10.6dBm to -9.3dBm. Because of lack of noise analyzer working at this high frequency band in our lab, noise figure vs phase states is simulated, as shown in Fig. 11 (b). The average NF is about 15.7dB. Finally, the performance summary and comparison is shown in Table I.

![Fig. 11. (a) Measured IP1dB vs phase states at 38GHz; (b) Simulated NF vs phase states at 38GHz.](image)

### Table I. Performance summary and comparison

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Process</th>
<th>Topology</th>
<th>Frequency (GHz)</th>
<th>Phase range (°)</th>
<th>Phase resolution (bit)</th>
<th>Average gain (dB)</th>
<th>RMS phase error (°)</th>
<th>RMS gain error (dB)</th>
<th>Input P1dB (dBm)</th>
<th>Power (mW)</th>
<th>Core area (mm²)</th>
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<tr>
<td></td>
<td>0.12um Bi-CMOS</td>
<td>ST</td>
<td>30~40</td>
<td>360</td>
<td>4</td>
<td>-13</td>
<td>4@35 GHz</td>
<td>1@35 GHz</td>
<td>5~6</td>
<td>0</td>
<td>0.12</td>
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<td>90nm CMOS</td>
<td>ST</td>
<td>57~64</td>
<td>360</td>
<td>5</td>
<td>-18</td>
<td>2~10</td>
<td>1.8</td>
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<td>0</td>
<td>0.34</td>
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<tr>
<td></td>
<td>0.13um BiCMOS</td>
<td>VS</td>
<td>15~26</td>
<td>360</td>
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<td>-4.6~3</td>
<td>6.5~13</td>
<td>1.1</td>
<td>-0.8</td>
<td>0</td>
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<tr>
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<td>360</td>
<td>6</td>
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<td>&lt;2</td>
<td>&lt;1.5</td>
<td>±1.1</td>
<td>0</td>
<td>±0.8</td>
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<tr>
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<td>360</td>
<td>10</td>
<td>-3.5~1</td>
<td>&lt;1.22</td>
<td>1.5</td>
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<tr>
<td></td>
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<td></td>
<td>-10.6</td>
<td>0</td>
<td>±0.8</td>
</tr>
</tbody>
</table>

ST: Switched Type; VS: Vector Summing; *with pads.
6 Conclusions
This paper has presented a 6-bit vector summing phase shifter in 0.13um SiGe BiCMOS process designed at 38GHz 5G frequency band. A linear gain adjustment VGA with modified gain control method is presented and is used in phase shifter for vectors weighting. Combined with the degenerated-Q QAF for accurate I/Q generation, high phase resolution and low RMS phase error are achieved with easy control. The phase shifter also has a compact size. These characteristics make the proposed phase shifter suitable for precise beam-steering and large-scale phased array integration in 5G mm-wave communication.

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