A 25-35 GHz 5-bit Digital Attenuator with Low RMS Amplitude Error and Low Phase Variation in 65 nm CMOS

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Abstract A mm-wave 5-bit digital attenuator with low RMS (root mean square) amplitude error and low phase variation is presented in 65 nm CMOS. The attenuator combines the PI/T-type topology with embedded switches and PI-type topology with the SPDT (single-pole-double-throw) switches to alleviate the insertion loss issue of the conventional PI/T-type topology with embedded switches in mm-wave frequency band, and achieves high attenuation range while maintaining compact chip size. The amplitude/phase calibration technique is proposed to reduce the RMS amplitude error/phase variation and improve the circuit robustness. The presented attenuator has been integrated in a Ka-band phased-array transmit front-end module and achieves 15.5 dB attenuation coverage with the step of 0.5 dB. The RMS amplitude error and RMS phase variation are 0.13-0.25 m dB if the operation frequency is limited to 26.9-31.4 GHz. The core chip size is 434 \(\mu\)m \(\times 360\ \mu\)m. The main contributions of this paper are summarized as follows.

1. Introduction

Phased-array systems have been extensively used in radar and satellite communications since they could achieve better signal-to-noise ratio, higher data-rate and higher channel capacity [1–4]. A phased array system contains many transmit/receive (T/R) front-end modules. The core functions of the T/R modules include signal amplification, phase shifting, and gain controlling [5–10]. Amplitude-controllable circuit plays a key role in phased-array systems. For amplitude control, the attenuator is preferable compared with variable gain amplifiers as it can achieve lower power consumption, lower control complexity and wider bandwidth [11–13]. In general, phased array system requires the attenuator to provide precise amplitude control (0.5 dB step in this work) and large attenuation range (15.5 dB in this work) with low insertion phase variation over the different attenuation states (<6° in this work). Generally, there are mainly three kinds of schemes to implement the attenuator. One is based on the basic type of PI-, T- topologies with embedded switches [14–19], as shown in Fig. 1 (a). This scheme is highly depending on the switch performance. The switch loss in CMOS is usually high due to the conductive substrate, even though the floating body technology can reduce the switch loss. Therefore, this scheme is mostly used in CMOS circuits with the operation frequency of under X band [14–16,18,19]. [20] adopts PI/T-type topology with the SPDT/DPDT (single-pole-double-throw/double pole double throw) and series inductors to improve the cascaded matching performance, result in lower insert loss across DC-20 GHz. However, it consumes more chip size. Besides, the attenuation value is sensitive to the load variation. The third scheme is the distributed attenuator [7, 21–25], while it still has troubles in the attenuation ranges since it demands many transmission lines and hence consumes a large chip area [21]. Moreover, previous works have rarely discussed the amplitude/phase calibration issues of the attenuator [14, 15, 20–22, 26], since numerous components in the PI/T type attenuator and transmission lines in the distributed attenuator are particularly troublesome to realize the calibration.

The main contributions of this paper are summarized as follows.

1) The attenuator combines the PI/T-type topology with embedded switches and PI-type topology with SPDT switches to alleviate the insertion loss issue of the conventional PI/T-type topology with embedded switches in mm-wave frequency band, and achieves high attenuation range while maintaining compact chip size.

2) Amplitude/phase calibration technique is proposed in the attenuator design, thereby improving the circuit ro-
busines and helping the attenuator achieve competitive performance compared with the state-of-the-art works.

This paper is organized as follows. Section II introduces the circuit design. In Section III, the measurement results are shown. Section IV presents the conclusions.

2. Circuit descriptions

Conventional attenuator consists of the basic 1-bit 0.5 dB, 1 dB, 2 dB, 4 dB and 8 dB attenuator stages in cascade. The process variations would have influence on the RMS amplitude error and phase variation in this case. This paper presents one amplitude calibration technique to reduce the amplitude error, which employs one different cascade strategy and extra amplitude calibration units to make the attenuation value tunable. The simulations show that the attenuator stages with 0.5 dB, 1 dB and 2 dB attenuation have small amplitude errors across 25-35 GHz in various process corners. By contrast, the attenuator stages with 4 dB and 8 dB attenuation can introduce ±0.5 dB amplitude error. Therefore, this paper splits 4 dB and 8 dB attenuation into 3.5 dB plus 0.5 dB attenuation and 7.5 dB plus 0.5 dB attenuation, respectively. The amplitude error could be manually calibrated by bypassing 0.5 dB calibration units if the measured attenuation value is higher than the desired value or cascading extra 1 dB calibration units if the measured attenuation value is lower than the desired value. Fig. 2 depicts the schematic of the proposed attenuator with amplitude/phase calibrations. The attenuator consists of three topologies:

1) Simplified T-type unit with embedded switch for 0.5 dB and 1 dB attenuation.
2) PI-type unit with embedded switch for 2 dB and 3.5 dB attenuation.
3) PI-type unit with the SPDT for 7.5 dB attenuation.

T-type unit has the priority since it achieves the attenuation using less components compared with the PI-type. In the T-type, the attenuation is realized by switching $S_T$ in Fig. 1 (a) from OFF to ON. Assuming that the switch parasitics are ignored, the resistance $R_{sT}$ and $R_{pT}$ can be written as follows:

$$R_{sT} = Z_0 \frac{1 - 10^\frac{A}{20}}{1 + 10^\frac{A}{20}} \quad (1)$$

$$R_{pT} = Z_0 \frac{2 \times 10^\frac{A}{20}}{1 - 10^\frac{A}{20}} \quad (2)$$

where $Z_0$ is the characteristic impedance, and $A$ is the attenuation value in dB. In 50-Ω systems, $R_{sT}$ and $R_{pT}$ are 1.44 Ω and 868.1 Ω, respectively, when $Z_0 = 50$ Ω and $A = -0.5$ dB. It can be seen that the ratio of the shunt resistor and the series resistor for 0.5 dB attenuation is approximately 602.85:1. Therefore, the switch $S_T$ for the reference state can be removed, since it can’t bypass the series resistors effectively. In this work, metal resistors are used to realize the series resistance. The insert loss caused by the series resistance can be ignored when $S_T$ is OFF. Simultaneously, when $Z_0 = 50$ Ω and $A = -1$ dB, $R_{sT}$ and $R_{pT}$ are 2.88 Ω and 433.34 Ω, respectively. Therefore, the 1 dB attenuator also adopts the simplified T-type topology [26].

The simplified T-type unit has trouble to achieve the 2 dB attenuation since the series resistance is 5.73 Ω, which cannot be ignored. Metal resistors for 5.73 Ω is not fit due to larger aspect ratio result in higher risk. However, the value is limited by the sheet-resistance in CMOS. PI-type unit with embedded switches is adopted in this work, the $R_{sPI}$ and $R_{pPI}$ can be written as:

$$R_{sPI} = Z_0 \frac{1 - 10^\frac{A}{20}}{2 \times 10^\frac{A}{20}} \quad (3)$$

$$R_{pPI} = Z_0 \frac{1 + 10^\frac{A}{20}}{1 - 10^\frac{A}{20}} \quad (4)$$

when the characteristic impedance $Z_0 = 50$ Ω and attenuation value $A = -0.5$ dB, $R_{sPI}$ and $R_{pPI}$ are 11.6 Ω and 436.2 Ω. The PI-type unit improves the minimum resistance value of the type from 5.73 Ω to 11.6 Ω, which can slightly alleviate the sheet-resistance issue in CMOS.

In addition, the shunt capacitors $C_{3pcal}$ and $C_{4pcal}$ in Fig. 2 are introduced to compensate the insertion phase variation caused by the process variations for realizing the manual phase calibration. Actually, the high-pass and low-pass RC network characteristics can increase and decrease the phase
respectively [25,27–30]. Therefore, the $C_{3cal}$ is shunted to the series resistor to provide the high pass characteristics. On the contrary, the $C_{3cal}$ provides the low pass characteristics, which can compensate the insert phase variation caused by process variations. Simultaneously, the PI-type unit with the embedded switch is applied to realize the 3.5 dB attenuation. The phase calibration in 2 dB and 3.5 dB can slightly affect the amplitude response of the unit. The amplitude error caused by the phase calibrations can be also corrected by the amplitude calibration units in this design.

Two schemes are usually utilized to realize the 8 dB attenuation, including the 8 dB PI-type attenuation unit with the embedded switch and two 4 dB PI-type attenuation units in cascade. However, the insert loss is high due to the worse matching performance caused by the switch parasitics in CMOS. [14] introduces the series inductor to improve the matching performance caused by the switch parasitics in embedded switch and two 4 dB PI-type attenuation units in this design. This paper makes a trade-off between the insert loss and chip size by adopting the PI-type unit with the SPDT chip area. The amplitude error of the unit is decreased significantly from 0.1-0.4 dB to 0.2-0.5 dB after the calibration, although the RMS amplitude error is deteriorated slightly from 0.1-0.4 dB to 0.2-0.5 dB after the calibration, respectively. In the corner of SS/−40 °C, although the RMS amplitude error is decreased slightly from 3.5–4° to 0.7 – 1.5°.

3. Measurement results

The attenuator has been designed and integrated in a Ka-band transmit front-end module, which is fabricated in 65 nm CMOS. The chip microphotograph is given in Fig. 6. The core chip area is 434 μm × 360 μm. The measurements are performed by on-wafer probing on the PCB test board. All attenuator states were measured using an Agilent N5245A vector network analyzer. The attenuator doesn’t consume DC power since it uses the passive topology.

Fig. 3 shows the simulated 5 basic attenuation states of the proposed attenuator and the simulated zero (reference) state of the conventional all embedded switch topology. The 7.5 dB attenuation unit uses the SPDT switch to improve the matching performance. Thus, the 0 dB reference state achieves 12.81 dB insertion loss at 30 GHz, which is improved by nearly 1.89 dB compared with the conventional all embedded switch topology. Fig. 4 and Fig. 5 show the simulated RMS amplitude error and phase variation in various process and temperature corners. The amplitude error of the 4 dB and 8 dB attenuation stages is decreased by manually reconfiguring the calibration units. The phase variation of the 2 dB and 4 dB can be decreased by manual reconfiguring the switched capacitors. The RMS amplitude error and phase variation are smaller than 0.5 dB and 2.5° over the 25-35 GHz after the calibration, respectively. In the corner of SS/−40 °C, although the RMS amplitude error is deteriorated slightly from 0.1-0.4 dB to 0.2-0.5 dB after the calibration, the RMS phase variation is decreased significantly from 3.5 – 4° to 0.7 – 1.5°.

Fig. 5. Simulated and measured attenuation RMS phase error.

Fig. 3. Simulated attenuation characteristics of the attenuation block in major attenuation states.

Fig. 4. Simulated and measured attenuation RMS amplitude error.

Fig. 7 shows the measured 32 attenuation states referring to the reference 0 dB state. The proposed attenuator achieves
Table I. Performance comparison with previous works

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Tech.(nm)</th>
<th>Topology</th>
<th>Freq.(GHz)</th>
<th>Step(dB)</th>
<th>States</th>
<th>RMS Amp. Err.(dB)</th>
<th>RMS Pha. Var.(°)</th>
<th>Loss(dB@GHz)</th>
<th>Area(mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
<td>180</td>
<td>Switch embedded</td>
<td>15-18</td>
<td>1</td>
<td>15</td>
<td>0.46-0.8</td>
<td>NA</td>
<td>NA</td>
<td>0.17**</td>
</tr>
<tr>
<td>[20]</td>
<td>130</td>
<td>Using SPDT/DPDT</td>
<td>DC-20</td>
<td>1</td>
<td>32</td>
<td>&lt;0.7</td>
<td>&lt;2.5</td>
<td>~10@20</td>
<td>0.5</td>
</tr>
<tr>
<td>[21]</td>
<td>65</td>
<td>Distributed</td>
<td>50-110</td>
<td>0.75</td>
<td>14</td>
<td>NA</td>
<td>&lt;5</td>
<td>5.6@50</td>
<td>0.38</td>
</tr>
<tr>
<td>[22]</td>
<td>180</td>
<td>BiCMOS</td>
<td>Distributed</td>
<td>22-29</td>
<td>57-64</td>
<td>0.49-0.51</td>
<td>1-4.7</td>
<td>7.9@29</td>
<td>0.94</td>
</tr>
<tr>
<td>[31]</td>
<td>130</td>
<td>BiCMOS</td>
<td>Switch embedded</td>
<td>DC-20</td>
<td>0.5</td>
<td>0.37</td>
<td>&lt;4</td>
<td>7.2@20</td>
<td>0.14</td>
</tr>
<tr>
<td>[32]</td>
<td>250</td>
<td>BiCMOS</td>
<td>Switch embedded</td>
<td>6-12.5</td>
<td>0.26</td>
<td>0.26</td>
<td>2.2-3.5</td>
<td>12.7@12.5</td>
<td>0.29</td>
</tr>
</tbody>
</table>

This work 65 Switch embedded & using SPDT 25-35 0.5 32 0.13-0.48 0.13-0.25 1.24-2.08 12.81@30 0.16

*When the operation frequency is limited to 25.9-31.4GHz
**Estimated according to the microphotograph.#Dual band.

4. Conclusion

This paper presents one 25-35 GHz attenuator in 65 nm CMOS. It combines the conventional PI/T topology with embedded switch and PI/T topology with the SPDT. The amplitude/phase calibration is presented to improve the circuit robustness. The proposed attenuator shows the RMS amplitude error of 0.13-0.48 dB and the RMS phase variation of 1.24 – 2.08° across the 25-35 GHz, which is attractive for signal amplitude control in wideband micro- and millimeter-wave communication and satellite communication systems.

Acknowledgments

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References


