A high efficiency CMOS RF rectifier for RF energy harvesting with dynamic self-body-biasing technique

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Abstract In this paper, a radio frequency (RF) rectifier is proposed for RF energy harvesting. The proposed rectifier adopts a dynamic self-body-biasing technique to modulate the threshold voltage of MOSFET. It can improve the power conversion efficiency (PCE) of the rectifier. Designed with SMIC 0.18µm CMOS standard process, simulation results indicate that the proposed rectifier has higher PCE than conventional cross coupled rectifier when the input power is larger than -14dBm. The PCE of proposed rectifier achieves 72.3% when the input power is -3.7dBm.

keywords: RF energy harvesting, RF rectifier, power conversion efficiency (PCE)

Classification: Energy harvesting devices, circuits and modules

1. Introduction

RF energy harvesting has been increasingly found in wide range of applications, such as wireless sensor networks (WSN) and wireless body area networks (WBAN) [1, 2]. In circuit systems, RF energy harvesting system can convert RF power to DC supply power. If the RF power is stable, the DC power will be permanently provided by RF energy harvesting system. In some applications, such as implantable medical devices, battery is not suitable. Because, it needs routine maintenance and the size of battery is relatively large [3, 4, 5, 6, 7, 8]. Therefore, RF energy harvesting is an attracting solution and can be fully or partially used as a replacement of battery.

RF-DC rectifier is a primordial circuit in RF energy harvesting. The performance of RF-DC rectifier dominates the vital parameter, power conversion efficiency (PCE), of RF energy harvesting systems [9, 10, 11]. The higher PCE of RF energy harvesting systems is, the more energy can be obtained. From another perspective, to obtain a certain amount of energy, the higher PCE of RF energy harvesting sys-
ment of PCE performance. Different from previous papers, in [22] the body terminals of MOSFET are statically biased, which means the bias voltages do not change during a period of input signal. And [23, 24, 25, 26] are based on the Dickson charge-pump topology. In this work, we proposed a novel dynamic self-body-biasing rectifier for RF energy harvesting. By properly adding biasing circuits on the body terminals of MOSFET, the PCE can be further improved. The remainder of this paper is structured as follows. Section 2 analyses the PCE of cross-coupled differential topology. Section 3 discusses our proposed rectifier. Section 4 presents the simulation results of our proposed topology. Finally, the entire work is concluded in section 5.

2. Power conversion efficiency analysis for cross-coupled differential rectifier

PCE of RF rectifier is defined as the ratio of the output power $P_{\text{out}}$ and the input power $P_{\text{in}}$. The input power is also the sum of output power $P_{\text{out}}$ and the loss of power $P_{\text{loss}}$ during rectification. The PCE can be expressed as follows.

$$ PCE = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}} \quad (1) $$

There are two main contributors for $P_{\text{loss}}$ [27, 28]. (1) The conduction loss between the source and drain due to the finite conducting resistance when the MOSFET is in forward biased condition $V_{\text{f}}$. (2) The reverse current when the MOSFET is under reverse biased condition $I_{\text{r}}$. Conducting resistance and reverse current of MOSFET can be calculated by following equations.

$$ R_{cs} = \frac{V_{DS}}{I_{DS}} = \frac{V_{DS}}{\frac{1}{2} \mu \nu C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2} \quad (2) $$

$$ I_{\text{r}} = I_0 \frac{W}{L} e^{\frac{V_{GS} - V_{th}}{\sqrt{2} \Phi}} (1 - e^{-\frac{V_{DS}}{\sqrt{2} \Phi}}) \quad (3) $$

Where, $R_{cs}$ is the conducting resistance of MOSFET in saturation region. In order to reduce conducting resistance, $V_{th}$ should be decreased. However, equation (3) indicates that decreasing $V_{th}$ will result a higher reverse current, which degrades the overall PCE performance. Things become worse when we use short channel MOSFET. Due to the drain-induced barrier lowering (DBL) effect, $V_{th}$ decreases when there is a relatively high voltage across the source and drain of MOSFET [29], leading to a higher reverse current. To address the challenges, we proposed a dynamic self-body-biasing rectifier. It can reduce both conducting resistance and reverse current of MOSFET by dynamically modulating $V_{th}$.

3. Proposed RF rectifier with dynamic self-body-biasing technique

According to the equations, threshold voltage can be modulated by its body voltage [30].

$$ V_{bN} = V_{b0N} + \gamma (\sqrt{2 \Phi_F} + V_{sb}) - \sqrt{2 \Phi_F} \quad (4) $$

$$ V_{bP} = V_{b0P} - \gamma (\sqrt{2 \Phi_F} - V_{sb}) - \sqrt{2 \Phi_F} \quad (5) $$

The simulation results of $V_{th}$ are shown in Fig. 4. Both $|V_{DS}|$ are set to 1.8V, and $W/L$ are 3.6$\mu$m/180n, 18$\mu$m/180n for NMOS and PMOS respectively. To individually bias body voltage of NMOS, it need to be fabricated in deep n-well. It can be seen that $|V_{th}|$ varies from approximately 0.1V to 0.9V when $V_b$ changes.

![Fig. 4. Simulation results of $V_{th}$ with different $V_b$.](image)

To evaluate the influence of body voltage on RF rectifier, Fig. 5 shows a RF rectifier with a DC voltage source, which can simulate the output voltage when the rectifier works in steady state. When RF rectifier is working in steady state, the output voltage is relatively constant. Because the load resistor and load capacitor form a high pass filter. $V_{in+}$ and $V_{in-}$ are two differential inputs, $V_{in+} = -V_{in-}$. $V_{dc}$ and $R_{load}$ are set to 1V and 1K$\Omega$ respectively. The performances of RF rectifiers can be evaluated through DC analysis. Fig. 6 presents the simulation $I_d - V_{in+}$ characteristics of $M_{p1}$. When $V_{in+}$ is less than -1V, the drain voltage of $M_{p1}$ is...
higher than 1 V, which means $M_{p1}$ should conduct current to the output. However, when $V_{in^+}$ is higher than -1 V, $M_{p1}$ should cut off. Under this situation, any current flow from the source to the drain is belong to leakage current, and it will degrade the overall PCE of the rectifier. It also indicates that when $V_b=1$ V, the conduction loss is less. While, the leakage current is less when $V_b=2$ V. In conclusion, if body terminal of PMOS is biased at higher voltage than source terminal, the MOSFET will have less leakage current. However, to reduce the conduction loss, the body voltage of PMOS should be same or slightly lower than source voltage.

Fig. 7 shows the circuits configuration of our proposed dynamic self-body-biasing rectifier. $M_{n1}$, $M_{n2}$, $M_{p1}$ and $M_{p2}$ consist the main rectifier. $M_{n3}$, $M_{n4}$, $M_{p3}$ and $M_{p4}$ generate a higher voltage $V_{bp}$ to drive the body biasing circuits. $V_{bp}$ is approximately equal to twofold of $V_{out}$. The body voltages of PMOS $V_{bp1}$ and $V_{bp2}$ are capacity coupling with input signals through capacitors $C_c$. $V_{bp1}$ and $V_{bp2}$ are limited by diodes $D_n$ and $D_p$ in the range of $V_{out} - V_{id}$ to $V_{bp} + V_{id}$. Where $V_{id}$ is the threshold voltage of diodes. Therefore, $V_{bp1}$ and $V_{bp2}$ are periodic signals from $V_{out} - V_{id}$ to $V_{bp} + V_{id}$ and have same phases with $V_{in^-}$ and $V_{in^+}$, respectively. The operation mechanism of dynamic self-body-bias is as follows. When $V_{in^+}$ increases and $V_{in^-}$ decreases, $M_{p2}$ is in reverse biased whereas $M_{p1}$ is in forward biased. Meanwhile, $V_{bp1}$ decreases with $V_{in^-}$ and $V_{bp2}$ increases with $V_{in^+}$. Based on the above analysis, both conduction loss of $M_{p1}$ and leakage current of $M_{p2}$ are reduced. Similarly, the same phenomenon will repeat when $V_{in^-}$ increases and $V_{in^+}$ decreases.

4. Simulation results and discussion

The dynamic self-body-biasing rectifier is designed with SMIC 0.18 $\mu$m CMOS technology. The RF input is a 915 MHz sinusoid. The dimensions of $M_{n1,2}$, $M_{p1,2}$ are $3.6 \mu m$, $18 \mu m$ respectively. In order to compare the performance of our proposed rectifier with conventional cross-coupled rectifier, the conventional cross-coupled rectifier is implemented with the same parameters. Fig. 8 shows the simulation results of PCE. Compared to conventional cross-coupled rectifier, the PCE of proposed rectifier is higher when input power is larger than -14 dBm. The explanation is as follows: When the input power is low, the power consumption of proposed rectifier becomes significant part of loss, because of the extra circuits. However, as the input power increases, the contribution of proposed dynamic self-body-biasing technique becomes dominant, which improves the PCE.
The performances of RF rectifiers in relevant literature are listed in Table I. The conventional cross coupled rectifier and multistages rectifier using low-threshold-voltage transistors are adopted respectively in [31], [32]. Benefiting from the dynamic self-body-biasing technique, the proposed rectifier has the highest PCE.

### Table I. Comparison with relevant literature

<table>
<thead>
<tr>
<th>Technology</th>
<th>Frequency</th>
<th>Load</th>
<th>PCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work</td>
<td>0.18 µm</td>
<td>5KΩ</td>
<td>72.3% @ -3.7dBm</td>
</tr>
<tr>
<td>ASSCC</td>
<td>0.18 µm</td>
<td>10KΩ</td>
<td>66% @ -12dBm</td>
</tr>
<tr>
<td>ICECS</td>
<td>0.13 µm</td>
<td>100KΩ</td>
<td>70% @ -17dBm</td>
</tr>
</tbody>
</table>

5. Conclusion

This paper proposes a dynamic self-body-biasing technique for RF rectifiers, which improves the PCE. A RF rectifier adopting this technique is designed with 0.18 µm CMOS technology. Simulation results show that the proposed technique can reduce both conduction loss and leakage current of RF rectifiers. Therefore, it is an effective method to improve PCE performance for RF rectifier.

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References


