Quenching Bias Circuit with Current mirror for Single Photon Detection

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Abstract To minimize the characteristic variation of SPADs (Single-Photon Avalanche Diodes) with bias, a current mirror based quenching bias circuit is implemented and tested for Single Photon Detection. With the proposed quenching bias circuit, the operational bias variation of SPADs is successfully reduced. A SPAD and quenching bias circuit are integrated in a 43 μm × 43 μm area to make a micro pixel. The optimized bias circuit maximizes the photon detection area to have more than 50% fill factor. This paper is based on a 0.18μm standard CMOS process with thick gate oxide option.

key words: SPAD (Single Photo Avalanche Diode), current mirror, quenching, fill factor, operation voltage

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

For single photon detections, traditionally photo multiplier tubes (PMTs) are utilized to amplify incident photon signal [1]. However, PMTs are rather large in size and require very high operating voltage (~ 1 kV or higher). Recently an array of APDs (Avalanche Photo Diodes) are utilized for the single photon detection. APDs [14]-[16], small in size and operating under relatively low voltage, have many advantages compared with PMTs. APDs are insensitive to magnetic field, which is a very important requirement for some applications such as PET (Positron Emission Tomography) when PET is integrated with MRI (magnetic resonance imaging). Also APDs have low electronic noise (high SNR) than PMTs [17]-[21]. For these reasons, for the application of single photon detection, APDs have become popular [2], [28]-[31].

APDs for single-photon detection, commonly made from the silicon, are used in an array [22]-[25]. Because theses single-photon avalanche photo diodes (SPADs) are operating in breakdown region, the characteristics such as breakdown voltage vary from one device to another. For SPADs using an array, the breakdown voltage variation leads to improper operations. If all the SPADs in an array are biased with the same voltage, the breakdown voltage variation would leads to different responses among SPADs. Some SPADs respond with a photon incidence, while other SPADs do not produce any signal since the bias is not enough to cause avalanche breakdown and the subsequent current multiplication.

SPADs are biased using a bias circuit as shown in Fig. 1, operating in Geiger mode. For Geiger mode operation, the bias across a SPAD should be larger than the breakdown voltage. SPADs in Geiger mode are in unstable state waiting a photon incidence. Once a photon is incident on a SPAD, avalanche breakdown occurs, and large current will follow [3]. Once the large current flows, the bias circuit reduces the bias across the SPAD to stop the breakdown operation, which is called quenching. Without the quenching, the breakdown current will flow indefinitely making SPAD useless for photon detection. After the quenching, the current through SPAD drops to very low level. Then the bias circuit restore the SPAD bias voltage to the original state for the next photon detection called reset [3]. For a proper operation, the bias across SPADs should be right, a little bit larger than the breakdown voltage. If the bias across an SPAD is far excess of the breakdown voltage, erroneous signals from self-breakdown, which are not related to photon incidence, are produced. The range of operation voltage applied to the anode in the case of Hamamatsu MPPC APD, for example, becomes -70 ~ -72 V or so [4], [26]-[27]. In this paper, the proposed circuit reduces the time difference caused by the breakdown voltage variation within 2 V. The range of breakdown voltage variation is similar to SPAD of Hamamatsu [4].

When we apply biases to many SPADs, applying bias with right amount of voltage is very difficult if the breakdown voltages of SPADs vary depending on the devices. In this paper, we propose on-chip SPADs using a standard CMOS process and the pairing bias circuit for single photon detection which can accommodate the breakdown voltage variation of many different SPADs, ensuring a proper operation.

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DOI: 10.1587/elex.16.20190657
Received October 25, 2019
Accepted November 1, 2019
Publicized November 18, 2019
2. Bias circuit architecture

Basic bias circuit (Fig. 1) adjusts the bias across a SPAD throughout a photon detection process. The bias across the SPAD is the difference between the cathode voltage ($V_S$) and the anode voltage ($-V_{LOW}$), i.e., $V_s + V_{LOW}$. For a given anode voltage $V_{LOW}$, the bias circuit modifies the cathode voltage, also called sensing node voltage, $V_S$ to change the bias across the SPAD for the single-photon detection process.

Fig. 1. Schematic of basic quenching circuit.

Fig. 2 shows the sensing node voltage ($V_S$ in Fig. 1) changes with time, when a photon is incident. The sensing node voltage maintains its high voltage ($V_{DD}$) when SPAD current is zero. Once a photon comes into SPAD, the sensing voltage decreases from the current flow through the SPAD and the bias circuit (passive quenching). The rate of voltage drop is slow during the passive quenching, since the current increase is rather slow after photon detections. Once the sensing node voltage ($V_S$) is below a certain level, the bias circuit turns a switch on to pull the sensing node voltage down almost to the ground (0 V), called active quenching. Though the quenching operation (both passive and active quenching, the SPAD bias becomes low and the avalanche breakdown stops. After the sensing node voltage becomes low around 0 V, hold-off state follows where the sensing node voltage remains low. Shortly after the hold-off, a reset operation restores the sensing node voltage to the original state ($+V_{HIGH}$). Once the sensing node voltage is restored, SPAD is in the breakdown region, and avalanche breakdown and large current flow is possible to detect the next photon incidence. All these operations (passive and active quenching, hold-off, and reset operations) are performed by the bias circuit. During these operations, the SPAD cannot detect a photon since it is not ready, called dead time. Most of research on quenching bias circuits focuses on reducing dead time and/or power consumption. However, at the same time, to minimize the effect of SPAD operation voltage variation is also very important to guarantee a proper operation.

Fig. 2. Voltage waveform of the sensing node ($V_S$ in Fig. 1) for a quenching bias circuit.

Fig. 3. Structure of SPAD. (a) P-N junction type and (b) deep N-well type.

SPADs used in this paper are ones made directly using a standard CMOS process, the structures shown in Fig. 3 (a) and (b). Fig. 3 (a) shows the SPAD of the P-N junction type, which has narrow depletion width to have a fast response time and a large gain. As a result, a fast response is expected.
Fig. 3(b) shows the SPAD of deep N-well type, which has a thick depletion width to have more photons absorbed, however the response speed is rather slow [5]. In this paper, the quenching circuit was integrated with the SPAD of both deep N-well type and P-N junction type. Even though SPADs are so much different in their structure, it will be shown in Fig. 8 that the bias circuit output is almost identical with the proposed bias circuit.

The schematic of resistor type quenching bias circuit is shown in Fig. 4. The sensing node voltage ($V_S$) is connected to $V_{HIGH}$ through a resistor. From this circuit topology, the sensing node voltage is $V_{HIGH}$ when no current flows. In such a case, the applied bias for SPADs in an array are all identical to $V_S + V_{LOW} = V_{HIGH} + V_{LOW} = V_{BR}$ (breakdown voltage) + $V_{EX}$ (excessive voltage). If there are breakdown voltage variation among SPADs since they are so many in numbers in an array configuration, the operation is susceptible to variation of SPAD characteristics. The monostable circuit, not shown in detail in this paper, turns on the reset transistor ($S_{RESET}$ in Fig. 3) to restore the sending node voltage to $+V_{HIGH}$, after the hold-off operation [6].

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Fig. 4. Resistor type quenching bias circuit [7].

Fig. 5. Proposed type quenching bias circuit.

The schematic of the designed quenching bias circuit is shown in Fig. 5. The proposed bias circuit has a current mirror to apply the sensing node voltage (shown in the left part of the schematic) and variable inverters for constant quenching time. The anode of SPAD is applied sufficiently low voltage to produce the avalanche breakdown. If a photon is incident, a avalanche photocurrent is produced. The amount of the photocurrent is compared with the constant amount of current by the current mirror. As a result of the avalanche current occurs on SPAD, the sense node voltage $V_S$ is lowered due to the increased current through the SPAD (passive quenching), then $M_S$ detects voltage drop to turn $M_O$ on. As a result, $V_S$ further drops to the minimum value and the low voltage is maintained (active quenching and hold-off). At the same time, the output of variable inverter is high to turn $M_R$ on and $M_O$ off. Then $V_S$ is changed to a high voltage to be ready for the next photon detection (reset). Even with the identically designed and manufactured SPADs, the characteristics are all different. The breakdown voltages can vary substantial from devices to devices, which also varies with temperature. Therefore the bias stabilization is very important to guarantee proper operation of SPADs. From the variations due to breakdown voltages, current flowing at cathode may be different if a constant voltage is applied across the SPAD. To minimize the operational variations from different SPADs, the operating bias is applied by a current mirror connected to the cathode of SPADs. By reducing the effect of the breakdown voltage variation, the quenching and reset time can be made more or less constant, therefore errors occurring during the photon detection process is reduced.

3. Simulation results

The simulation results of the resistor type quenching bias circuit are shown in Fig. 6. The maximum operating speed target of quenching circuit is 50 MHz. All circuit is designed so that dead-time can be operated to about 10 ns in order to achieve target, and this is confirmed by simulation results. When $V_{LOW}$ changes from $-V_{BR}$ to $-(V_{BR} + 2 V)$, the different time response can be observed. The time variation of quenching start time is about 1.6 ns when $V_{LOW}$ varies from $-V_{BR}$ to $-(V_{BR} + 2 V)$. On the other hand Fig. 7 shows the simulation result of the proposed circuit. The proposed circuit demonstrated the time variation of only 196 ps for the same $V_{LOW}$ variation from $-V_{BR}$ to $-(V_{BR} + 2 V)$. In summary, the proposed circuit (Fig. 5) exhibit only 10% time variation of that of the conventional resistor type quenching bias circuit.

Fig. 6. $V_S$ node transient simulation results of the resistor type quenching bias circuit.
4. Experimental results

Both the resistor type quenching circuit and the proposed quenching bias circuit (Fig. 5) are fabricated with on-chip SPADs using a 0.18 µm TSMC CMOS process. The layout of the proposed quenching bias circuit with an SPAD (a micro pixel) is shown in Fig. 8. This micro pixel size is 43 µm × 43 µm (bias circuit only 13 µm × 43 µm). The size of SPAD within the pixel is important to maximize photon detection probability. A micro pixel, composed of a SPAD and the bias circuit, is the basic unit of the array. Fig. 9 shows the layout of the bias circuits. Comparing the layout of the proposed quenching bias circuit (Fig. 9 (a)) with the resistor type quenching bias circuit in a micro pixel (Fig. 9 (b)), the proposed circuit area is only 33 % of the resistor type circuit. The fill-factor which is the ratio of SPAD area to the total area can be improved with the proposed circuit. In addition, it is possible to increase the size of SPAD in a micro pixel, increasing the probability of the photon detection. Fig. 10 shows fabricated chip and the layout of the proposed bias circuits with SPADs. For SPADs, the size and the types are all different. Five pixels on the left side use the SPAD of Deep N-well type as shown in Fig. 3(b), The other five pixels on the right side use the SPAD of P-N junction type as shown in Fig. 3(a). The opening area of each SPAD reduces from left to right gradually to achieve different characteristics.

The measurement setup is as shown in Fig. 11 and Fig. 12. The array of micro pixels are tested in a dark chamber. A commercial yellow LEDs (light emitting diodes) are used to illuminate the micro pixels. The outputs of the bias circuit are monitored using an oscilloscope (LeCroy Wavesurfer 454). The light from the LED was pulsed and measured using an illuminance meter (Konica Minolta T-10). Incidence time of photon is determined by power per unit area of light source and area of the SPAD. Following equations (1) and (2) show process for injecting a single photon into SPAD. First, illumination is divided by typical luminous efficacy of light source, and power per unit area is obtained as shown in equation (1).

\[
\text{Power} = \frac{\text{Illuminance}}{\text{Typical luminous efficacy of a light source}} \quad (1)
\]

The number of photons can be obtained as shown in Equation (2) by multiplying the power per unit area obtained, area of SPAD, photon incidence time and dividing by energy of single photon.

\[
\text{Number of photons} = \frac{\text{Power} \times \text{Area of SPAD} \times \text{photon incidence time}}{\text{Energy per photon}} \quad (2)
\]
The energy of single photon is 2.2 eV, which is $3.5 \times 10^{-19}$ J. The area of the SPAD is $43 \mu m \times 30 \mu m$ as shown in Fig. 8. Order to apply a single photon to SPAD, photon incidence time was set to 10 ns repeated every 100 ns (10 MHz) by illuminance of light source. Therefore, the input light pulse roughly contains a small number of photons, close to a single photon per incidence time. The simulation was based on the $V_S$ node. However, in the actual measurement, in order to perform the $V_S$ node measurement, a PAD must be added, which increases the capacitor component and it is negatively affects the performance of the SPAD and the circuit. The output of the quenching circuit is similar to the operation of a $V_S$ node, avoiding the aforementioned phenomenon. Despite the addition of the PAD, the output of the quenching circuit is almost unaffected by the capacitor component, which does not adversely affect circuit operation. Therefore, the result is similar to $V_S$ node. In the actual measurement, the output node was measured based on this principle, and the resistor type was compared with the result of the proposed circuit.

Fig. 13 shows the measurement results of the resistor type quenching circuit to be compared. The red pulse is the light source. As shown in Fig. 12 (a), the yellow LED is applied 10 ns per 100 ns, and the yellow pulse is the output of the quenching circuit. When $-(V_{BR} + 2)$ V is applied to $-V_{LOW}$, the anode of the SPAD, the time difference between the light source and the output is 5.1 ns. If $-(V_{BR})$ V is applied, the time difference is 7.2 ns. The time difference of SPAD variation in resistor type is about 2.1 ns. Fig. 14 shows the measurement results of the proposed circuit. The resistor type and the measurement conditions are the same. When $-(V_{BR} + 2)$ V is applied to $-V_{LOW}$, the time difference between the light source and output is 5 ns. The time difference when $-V_{BR}$ V is applied to $-V_{LOW}$ is 5.2 ns, and the time difference by SPAD variation is about 200 ps.

5. Conclusion

This paper presents a micro pixel array for photon detector with the proposed quenching bias circuit. Even with the same type of SPAD, they have operation voltage variation from temperature, for example, causing the time variation in the quenching circuit. The proposed design reduces time difference. The time variation is only about 196 ps in simulation and about 200 ps in experimental results with $-V_{LOW}$ variation from $-V_{BR}$ to $-(V_{BR} + 2)$ V. In addition the bias circuit size is reduced to achieve more than 50% fill-factor to increase the sensitivity of the device.

Acknowledgments

This research was supported National Research Foundation of Korea Individual Basic Science & Engineering Research Program (NRF-2018R1D1A1B07049663), and by the MSIT(Ministry of Science and ICT), Korea, under the
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