High frequency and high efficiency DC-DC converter with sensorless adaptive-sizing technique

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Abstract A high frequency and high efficiency DC-DC converter with sensorless adaptive-sizing technique is proposed. Instead of conventional adaptive-sizing technique with current sensor, the proposed converter estimates the load current according to the output voltage of error amplifier for switch scaling. The elimination of current sensor reduces power consumption, thus improving efficiency further. This design is validated through simulation in a 0.18 μm CMOS process. At switching frequency of 150 MHz and light-load of 20 mA, the proposed converter achieves a high efficiency of 82.4%, while it is 73.7% with conventional adaptive-sizing technique, and 62.4% without adaptive-sizing technique.

key words: DC-DC converter, high frequency, light-load efficiency, adaptive-sizing, sensorless

Classification: Integrated circuits

1. Introduction

In DC-DC converters, light-load efficiency which is highly related to battery lifetime for portable devices, is much lower than heavy-load efficiency due to the higher ratio of power loss to output power at light-load [1, 2, 3, 4]. On the other hand, DC-DC converters with high switching frequency at tens or hundreds of megahertz have obtained wide research attention, due to their advantages of high integration level and high power density [5, 6, 7, 8]. However, high switching frequency also increases switching loss and harms efficiency especially light-load efficiency [9, 10, 11, 12]. Therefore, efficiency improvement is more strongly required for light-load and high frequency applications [13, 14, 15, 16]. Adaptive-sizing technique is presented as an efficient way to improve light-load efficiency [17, 18, 19]. It usually utilizes a current sensor to sample the load current for power transistor size selection [20, 21, 22]. However, introducing current sensor suffers from power loss and circuit delay, which is more serious for high efficiency and high frequency applications [23]. To improve the efficiency while not sacrificing other performance of DC-DC converter, a novel and simple method of sampling load current is proposed in this letter. This method estimates the load current according to the output voltage of error amplifier, rather than by current sensing circuit.

2. Conventional adaptive-sizing technique with current sensor

At light-load condition, DC-DC converter is often operated in discontinuous conduction mode (DCM) [24, 25, 26]. For DCM converter, the switching loss of power transistor $P_{sw}$ can be expressed as

$$P_{sw} = C_{gate}V_{DD}^2f_{sw}. \quad (1)$$

where $C_{gate}$ is the total capacitance of power transistors and their drivers, $V_{DD}$ is the supply voltage and $f_{sw}$ is the switching frequency.

And the conduction power loss $P_{cond}$ is given by

$$P_{cond} = I_L^2(D_1R_{on,p} + D_2R_{on,n} + R_L). \quad (2)$$

where $I_L$ is the average inductor current, $D_1$ and $D_2$ are the duty cycles of increasing and decreasing inductor current respectively, $R_{on,p}$ and $R_{on,n}$ are the on-resistances of power transistors PMOS and NMOS, and $R_L$ is the equivalent series resistance (ESR) of inductor.

It can be seen that both $P_{sw}$ and $P_{cond}$ are relative to the sizes of power transistors. Specifically, $C_{gate}$ and hence $P_{sw}$ are proportional to transistors widths, while $R_{on,p}$ and $R_{on,n}$ are inversely with transistors widths. Therefore, the optimum widths of transistors are existed to balance $P_{sw}$ and $P_{cond}$, thus making the total power loss minimum. Since the optimum widths of transistors are proportional to load current which will be shown in next section, adaptive-sizing technique is implemented by selecting the optimum widths of transistors at different loads. Conventional adaptive-sizing technique usually utilizes current sensor to sample the load current, which increases both power loss and circuit delay.

3. The proposed sensorless adaptive-sizing technique

A buck converter based on the proposed sensorless adaptive-sizing technique is shown in Fig. 1. This design estimates the load current by comparing the output voltage of error amplifier $V_{ea}$ with three reference voltages $V_{ref1} \sim V_{ref3}$, then...
adaptive-sizing logic selects the optimum group of transistors according to the comparison results. Meanwhile, a high accuracy delay-compensated ramp generator similar to the one in [27] is used for high frequency application, and a DCM control block is added to guarantee DCM operation.

![Diagram](image)

**Adaptive-sizing technique**

Fig. 1. Buck converter based on sensorless adaptive-sizing technique.

Considering the complexity of design and the larger current per unit width of NMOS power devices, only the sizes of PMOS devices and their drivers are optimized in this work. So only the conduction loss of PMOS transistor $P_{cond,p}$ is taken into account

$$P_{cond,p} = \frac{I^2_{PMOS}}{\mu_p C_{ox} W_p (V_{DD} - V_{TP})}. \quad (3)$$

where $I_{PMOS}$ is the root mean square (RMS) current in the PMOS transistor, $\mu_p$ is the hole mobility, $C_{ox}$ is the gate oxide capacitance per unit area, $W_p$ and $L$ are the width and length of the PMOS transistor, and $V_{TP}$ is the threshold voltage of the PMOS transistor.

It can be calculated that the approximate optimum width $W_{p,\text{opt}}$ is

$$W_{p,\text{opt}} = \frac{I_{PMOS}}{C_{ox} V_{DD}} \sqrt{\frac{1}{\mu_p (V_{DD} - V_{TP}) f_{sw}(1 + \frac{1}{f} + \frac{1}{f^2} + \cdots)}}. \quad (4)$$

where $f$ is the fan-out factor of the tapered buffer design. From Eq. (4), the optimum width of PMOS transistor can be scaled proportionally to $I_{PMOS}$, and also to the load current $I_o$. Since adaptive-sizing is mainly used to improve light-load efficiency [28, 29, 30], the value of $I_o$ in DCM should be estimated for switch scaling.

Actually, as Fig. 2 shows, the variation of $I_o$ yields different steady state values of $V_{ea}$ in DCM, while it does not stand in continuous conduction mode (CCM). Furthermore, the duty cycle $D_1$ in CCM buck converter is

$$D_1 = \frac{V_o}{V_{in}}, \quad (5)$$

which means that $D_1$ only depends on input voltage $V_{in}$ and output voltage $V_o$, and it is irrelevant to load current. Instead, the duty cycle in DCM buck converter is expressed as

$$D_1 = \frac{2LV_o I_o}{V_{in}(V_{in} - V_o)T}. \quad (6)$$

where $L$ is the inductor and $T$ is the switching period. It means that $D_1$ is determined not only by $V_{in}$ and $V_o$, but also by $I_o$. Therefore, with varied load currents, different values of $D_1$ are obtained by regulating $V_{ea}$, thus regulating the position of the intersection point between $V_{ea}$ and the ramp signal. Specifically, larger $I_o$ means larger $D_1$ and larger $V_{ea}$, as Eq. (6) and Fig. 2(b) show. Hence, the value of $I_o$ can be estimated indirectly according to $V_{ea}$, for establishing the optimum width $W_{p,\text{opt}}$.

![Plots](image)

**Fig. 2.** Plots of main signals at steady state with different $I_o$ (a) in CCM, (b) in DCM.

In this design, by comparing $V_{ea}$ with three reference voltages $V_{ref1} \sim V_{ref3}$ ($V_{ref1} < V_{ref2} < V_{ref3}$), four sizes of PMOS transistors 1X, 4X, 7X and 10X are scaled. When $V_{ea}$ is larger than $V_{ref3}$ which means heavy load and CCM operation, the PMOS transistor is scaled as 10X. When $V_{ea}$ is less than $V_{ref3}$ which means light load and DCM operation, it is re-compared with $V_{ref1}$ and $V_{ref2}$, to choose the optimum size among 1X, 4X and 7X. This method of indirectly estimating the load current is appropriate here, since the
load current is used only to choose the corresponding size of transistor in adaptive-sizing technique, and its accuracy requirement is not stringent.

4. Circuit implementation and simulation results

In this work, a 150 MHz switching frequency, 1.8 V input voltage and 1.2 V output voltage buck converter with the proposed adaptive-sizing technique is designed and simulated in a 0.18 µm CMOS process. The simulated plots of main signals are shown in Fig. 3, which are the load current $I_o$, the output voltage of error amplifier $V_{ea}$, the gate signals $V_{PG}$ of three PMOS transistors whose widths are 2 mm, 6 mm, 12 mm, and the output voltage $V_o$ respectively. It can be seen that $V_{ea}$ varies proportionally with $I_o$, and switch scaling is implemented according to the value of $V_{ea}$. At light load condition, only the transistor with 2 mm width is turned on, thus the total size of PMOS is 2 mm. For heavier loads, the total size of PMOS becomes $8 (= 2 + 6)$ mm, $14 (= 2 + 12)$ mm and finally $20 (= 2 + 6 + 12)$ mm. In this way, by configuring the three transistors, four sizes 1X, 4X, 7X and 10X are realized.

![Fig. 3. Simulated waveforms of main signals in designed converter.](image1)

Three buck converters which respectively apply the proposed sensorless adaptive-sizing technique, conventional adaptive-sizing technique with the current sensor in [28] and no adaptive-sizing technique are simulated in Fig. 4. Compared with the other two converters, the light load efficiency at 20 mA is improved by 8.7% (73.7% to 82.4%) and 20% (62.4% to 82.4%) with the proposed technique. A peak efficiency of 89.2% occurs at load current of 260 mA. Furthermore, the efficiency can maintain constant over a wide range of load current. The comparison results with previous works are listed in Table I. The results demonstrate that the proposed converter has a higher efficiency under light-load condition.

![Fig. 4. Plots of efficiency versus load current in different converters.](image2)

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<th>Table I. Performance comparison with previous works</th>
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*simulation results

5. Conclusion

This letter proposes a DC-DC converter with sensorless adaptive-sizing technique. The elimination of current sensor saves power loss and reduces circuit delay, which makes it more preferable for high efficiency and high frequency applications. Simulation results show that the efficiency can be improved up to 20% with a load current of 20 mA, by the proposed technique.

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References


