A 25-Gb/s High-Sensitivity Transimpedance Amplifier with Bandwidth Enhancement

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Abstract A 25-Gb/s transimpedance amplifier (TIA) is proposed and realised in a 0.18-μm SiGe BiCMOS process. A series-peaking network and a shunt-peaking network are used to increase the bandwidth of the modified TIA. A gain boosting circuit is used to optimize the input-referred noise. The chip occupies an area of 0.8mm², and consumes 82mW from a 3.3-V supply. The TIA transimpedance gain is ~4.5k ohms. Bit error rate tests indicate that the sensitivity of the fabricated TIA is -13 dBm for a date rate of 25.78125-Gb/s (Bit error rate (BER) = 10^-12, λ = 1310nm, ER=4.2dB, and 0.8 A/W PD responsivity).

key words: transimpedance amplifier, sensitivity, optical-electrical eye diagram, bandwidth enhancement.

Classification: Integrated circuits

1. Introduction

With the continuous growth of data volume due to increased cloud computing services, it is necessary to have high-speed telecommunication systems such as 25-Gb/s optical-fibre-link applications. In a conventional optical-fibre-link communication system, the laser is driven by a driver or a modulator and outputs an optical signal to a receiver through an optical fibre. At the receiving end, a photodiode (PD) detects the optical signal and generates a weak current signal, which is subsequently transformed by a transimpedance amplifier (TIA) to a voltage signal [1, 2,3]. The optical input power of the receiver varies over a wide dynamic range, which depends on the variations of the transmission distance, transmitted laser power, loss of the fibre, and efficiency of the PD [4, 5, 6, 7, 8, 9,10]. An automatic gain control (AGC) circuit, which varies the transimpedance gain, has been widely used to prevent the TIA from being overdriven at high input power, leading to improvements in jitter behaviour and sensitivity [11,12,13,14].

For high-speed TIA, achieving maximum bit rates requires a flat response of the magnitude of the transimpedance within the frequency range of interest. The use of networks, such as T-coil peaking, shunt-series peaking, shunt-peaking, and π-type peaking, have been reported to increase the bandwidth and remove the passband ripple [15,16,17,18,19,20,21,22,23,24,25, 26, 27, 28, 29, 30]. However, the bondwire inductance and the parasitic capacitance of the PD vary from chip to chip in engineering applications; thus, the TIA should be designed to be robust to these variations.

In this paper, a 25-Gb/s TIA is proposed and realised in a SiGe BiCMOS process. A series-peaking network and a shunt-peaking network are used to increase the bandwidth of the modified TIA. The passband ripple of the TIA is removed by optimising the locations of the pole-zero points and the resonant frequencies.

2. Circuit implementation

The block diagram of the proposed TIA is shown in Fig. 1. The regulator generates a regulated voltage to drive the PD, the phase splitter, and the driver. The first stage of the TIA is a single-ended transimpedance stage. This stage is optimised to achieve good noise. The AGC function is performed by a shunt resistor. The phase splitter (PS) converts the single-ended signal into a differential signal. A DC-offset compensation circuit is used to remove the output offset voltage to improve the input sensitivity performance. Only three amplifier stages are used in the high-speed channel of the TIA, resulting in low-power consumption.

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2.1 Input stage and bandwidth enhancement

A typical transistor implementation of the feedback TIA is shown in Figure 2(a). The inductive output impedance may lead to ringing if the circuit drives substantial load capacitance. To alleviate the stability issue, the circuit is modified as shown in Figure 2(b) [31]. In the high data rate transmission, placing the source follower Q3 outside the feedback loop may increase the power consumption and area.

The schematic of the proposed modified TIA input stage with a gain boosting technique and main noise sources is shown in Figure 3(a). The shunt-feedback topology is used as the input transimpedance stage because of its superior noise performance as compared with the common-base topology. The cascode topology is used to reduce the input-referred Miller capacitance to only ~2Cb when the transconductances (gm) of Q1 and Q2 are equal. The output of the shunt-feedback stage is taken from the collector of Q2, instead of the emitter of Q3, to alleviate the stability issue. Compared with the driving impedance at the output of the emitter follower Q3, this topology has higher driving impedance at the output node. A PMOS cascode current source is added in parallel with Q2 and RL to provide part of the bias current drawn by the input transistor Q1.

\[ i_{n,TIA} \approx \frac{4kT}{R_F} + \frac{4kT}{R_F}g_{m,Q1}^2 \left( \frac{1}{2g_{m,Q1}^2} + \frac{1}{R_L} \right) + \frac{\gamma g_{m,M1}}{R_L} \]

where \( g_{m,Q1} = I_{C,Q1}/V_T \). The -3dB bandwidth of the second order TIA is equal to [31]

\[ f_{-3dB} \approx \frac{\sqrt{2g_{m,Q1}R_L}}{2\pi RC_I} \]

Usually, \( f_{-3dB} \) bandwidth is set to 0.7 of the bit rate. The value of \( R_L \) can be increased while maintaining the same voltage drop as the case without the PMOS cascode current source. As shown in (1) and (2), the value of \( R_L \) decreases, the value of \( R_F \) increases, thus, the input noise current \( i_{n,TIA} \) decreases. The noise contributed by M1 can be decreased by using a long-channel transistor. To summarize, the input-referred noise is optimized by using the gain boosting technique.

In Figure 3(b), a shunt-peaking network (L_s) and an L-C low-pass filter (C_{PD}, L_B, C_{PAD}, L_1, C_1) are designed to have a frequency response that enhances the TIA’s bandwidth and reduces its input-referred noise current [32]. C_{PD}, L_B, and C_{PAD} are the parasitic parameters. L_1 is an on-chip inductance. The resonant frequency of the shunt-peaking network and L-C low-pass filter should be optimized to increase the bandwidth.

Figure 4 shows the simulation results of the
transimpedance gains under different test conditions. The results show that the series-peaking inductor \( L_B \) enhances the bandwidth, whereas the shunt-peaking inductor \( L_L \) removes the passband ripple. The shape of the TIA frequency response is based on the placement of the pole point, zero point and resonant frequencies [33, 34]. The required locations of these pole-zero points and resonant frequencies can be optimised by the TIA designer to remove the passband ripple. In addition, it shows that the bondwire at the TIA input should be optimized to guarantee a proper bandwidth [34].

2.2 AGC circuit
The simplified schematic of the proposed AGC is shown in Figure 5. The proposed AGC circuit utilises NPN transistor Q1 as a shunt resistor to broaden the dynamic range of the input current. NPN transistor Q1 acts as a shunt resistor. Its resistance value is calculated as

\[ R_{age} = \frac{1}{g_{m,q1}} = \frac{V_T}{i_c}. \]  

where \( i_c \) is the collector current of NPN transistor Q1. \( R_{age} \) decreases with the optical input power. The DC bias current of NPN transistor Q1 flows into the ground through transistor \( M_{E1} \).

2.3 DC-offset compensation
High-gain amplifiers require a DC-offset compensation to achieve high input sensitivity. Figure 6 shows the DC-offset compensation loop in the proposed TIA. The forward gain \( A_1 \) is the gain of the post amplifier that amplifies the total input-referred offset. The average value at the output of \( A_1 \) is measured by using an RC low-pass filter in the feedback loop. Thus, the DC component present at node \( V_{in} \) is replicated at the output \( A_3 \), and then the DC component present at node Vin is removed. The high-pass cut-off frequency is calculated as

\[ f_c = \frac{A_1 A_2}{R_C}. \]  

Usually, \( A_3 \) is less than unity and \( A_2 \) is large enough to remove the offset. The DC-offset would be clear that if the gain \( A_2 \) is infinite.

3. Experimental results
The proposed TIA is fabricated in a 0.18-\( \mu \)m SiGe BiCMOS process. The silicon area is 0.8 mm\(^2\). The proposed TIA is measured by incorporating a 25-Gb/s P-i-N photodiode to form a receiver optical subassembly (ROSA). The photo of the ROSA is shown in Figure 7.

The responsivity of the P-i-N photodiode is \( \sim \) 0.8 A/W. The prototypes of the ROSA are tested up to 25-Gb/s.
with a $2^{31-1}$ pseudo random binary sequence (PRBS) input patterns. The PRBS input is generated with a bit error tester SL3010A, which is a high-performance error detector with built-in code type generator and error code detector.

Figure 8 shows the measured electrical eye diagram at the output of a limiting amplifier which is used to amplify the output voltage of the proposed TIA when the optical input power is −16 dBm, wherein the rise time, the fall time, and the p-p jitter are 29.4ps, 29.0ps, and 14.2ps, respectively.

![Figure 8](image)

**Fig. 8** The measured electrical eye diagrams at the output of a limiting amplifier which is used to amplify the output voltage of the TIA, when the optical input power is −16 dBm.

Figure 9 shows the bit error rate (BER) performance of the fabricated TIA versus the input average optical power. Three prototypes of the ROSA are measured under −40°C, 25°C, and 85°C, respectively. The P-i-N photodiodes of ROSA is manufactured by the San’an optoelectronics CO., LTD. The responsivity of the P-i-N photodiodes of ROSA is ~ 0.8 A/W, and the extinction ratio of the transmitter is 4.2 dB. The minimum input optical power at which the TIA can maintain a BER of $10^{-12}$ is -17 dBm. Work with the increase of temperature, the BER increase gradually. At 85°C, the maximum input optical power at which the TIA can maintain a BER of $10^{-12}$ is -13 dBm. As shown in (1), the input noise current is mainly determined by the thermal noise of resistors and transistors, thus, the BER performance has large temperature dependence.

![Figure 9](image)

**Fig. 9** The Bit Error Rate (BER) performance of the fabricated TIA vs input average optical power.

Table 1 gives the measured differential gain of 4 prototypes of the ROSA versus input average optical power. The transimpedance gain is ~ 4.5K ohms when the input optical power is less than -14 dBm. When the input optical power is larger than -14 dBm, the value of...
the shunt resistor in Figure 7 will decrease with the input optical power to decrease the transimpedance gain. When the input optical power is 3.45 dBm, the gain is only 120 ohms. Table I summarizes the performances of this TIA relative to the prior works. The sensitivity in this work is less than -13dBm which is better than that of the prior works.

Fig. 10 The transimpedance gain vs input average optical power.

4. Conclusion

A 25-Gb/s high-sensitivity TIA with AGC is presented herein. The input stage of TIA is modified to alleviate the stability issue. Details of the various blocks of the circuit design are discussed. The optical sensitivity and the AGC functionalities of the fabricated TIA are verified by measuring optical-electrical eye diagrams. The measured results indicate that the proposed TIA can be used in the 25-Gb/s optical-fibre-link applications.

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References


