LETTER

A 0.88-pJ/bit 28Gb/s quad-rate 1-FIR 2-IIR decision feedback equalizer with 21dB loss compensation in 65nm CMOS process

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Abstract This paper describes quad-rate 1-FIR 2-IIR decision feedback equalizer (DFE) with summer reduction technique for high-speed serial communication in a 65nm CMOS technology. The proposed DFE halves the number of summers by using resettable slicer and summer with multiplexer. Therefore, the proposed DFE reduces power consumption significantly because summer dissipates a lot of power. The DFE that is verified by pre-layout simulations achieved 0.69 unit-interval (UI) eye-opening. The proposed DFE that is designed with a 65-nm technology operates at 28Gb/s and occupies 0.023mm². Finally, the power efficiency of the proposed DFE is 0.88-pJ/bit.

Key words: Receiver; High-speed wireline; Decision feedback equalizer; Infinite impulse response filter; Low power;

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

As high-speed wireline communication is grown, the data-rate has increased incredibly [1, 2, 3, 4]. Thus, inter-symbol interference (ISI) becomes more severe as the signal is distorted due to channel bandwidth limitation [5, 6]. Consequently, the demand for the performance of equalizers to remove the ISI caused by channel loss has also increased [7]. The continuous-time linear equalizer (CTLE) has been widely implemented to remove the ISI in high-speed serial links [8, 9, 10, 11, 12]. The CTLE compensates signal distortion without using a sampling clock. However, the CTLE amplifies both signal and noise, causing signal-to-noise ratio (SNR) degradation. Therefore, the DFE has been proposed to eliminate long-tail ISI without amplifying noise [13, 14, 15, 16, 17, 18, 19, 20, 21]. The non-linear equalizers are classified into two types: loop-unrolling DFE and n-tap direct finite impulse response (FIR) DFE. The conventional half-rate loop-unrolling DFE is shown in Fig. 1(a). The loop-unrolling DFE alleviates strict 1UI timing constraints caused by critical path in DFE [14, 15, 16]. However, loop-unrolling DFE requires more summers and d flip fl-

Fig. 1. Conventional half-rate (a) loop-unrolling DFE (b) n-tap direct FIR DFE

ops than n-tap direct FIR DFE, so loop-unrolling DFE consumes more power. The half-rate n-tap direct FIR DFE that is shown in Fig. 1(b) also consumes a lot of power as the number of taps increases to remove ISI [4, 17]. So, infinite impulse response (IIR) DFE has been reported to mitigate power penalty [18, 19, 20, 21, 22]. The IIR filter replaces the multiple discrete taps to reduce active area and power consumption.

In this paper, the quad-rate 1-FIR 2-IIR DFE with summer reduction technique is proposed. A typical quad-rate DFE has four summers that consume a lot of power. Therefore, we presented a low-power hybrid DFE that is implemented by resettable slicer and summer with multiplexer. The proposed DFE achieved a power reduction by 33% compared to a typical quad-rate DFE. The proposed low-power hybrid DFE that is verified by pre-layout simulations occupies 0.023mm². Finally, the power efficiency of the proposed DFE is 0.88-pJ/bit.

The organization of the paper is as follows. Section 2 presents the architecture of the proposed DFE. The circuit implementations are shown in Section 3. The simulation results are presented in Section 4, conclusions follow in Section 5.

2. Proposed DFE Architecture

The overall architecture of the receiver is shown in Fig. 2. The receiver consists of a CTLE to test the performance of the proposed DFE and the proposed DFE. The differential signals have been expressed as single-ended for simplicity. The proposed DFE is composed of the ev-

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Fig. 2 Overall architecture of the receiver

Fig. 3 The proposed 1-FIR 2-IIR hybrid DFE with summer reduction technique

en path and odd path. Even path is sampled by CLK0 and CLK180, odd path is sampled by CLK90 and CLK270. A typical DFE has summers depending on the number of interleaves (shown as a gray line in Fig. 2) [4, 18, 19, 20, 23, 24, 25]. The proposed DFE halves the number of summers by using resettable slicer and summer with multiplexer. The resettable slicer operates when clock is high, so the resettable slicer has low power consumption. The multiplexer is implemented by stacking the transistor. So, the multiplexer operates without additional power consumption. Therefore, the proposed DFE has a simple structure and reduces power consumption and active area. Fig. 3 illustrates the block diagram of the proposed 1-FIR 2-IIR hybrid DFE with summer reduction technique. The proposed DFE consists of two summers, slicers, latches, d flip-flops, and two IIR filters. The α_1 and α_2 are muxed of S0 and S180, and S90 and S270, respectively. Consequently, the FIR tap of the two phases is eliminated with one summer by muxing

Fig. 4 Timing diagram

Fig. 5 Schematic of summer with multiplexer in even path

output of the slicer. Because current-mode logic (CML) summer consumes a lot of power [3, 26, 27], the proposed DFE significantly reduces power consumption with the summer reduction technique. The timing diagram of the proposed DFE is shown in Fig. 4. S0 is sampled when CLK0 is high and reset when CLK0 is low. The rest of the phases are the same. Thus, the signals α_1 and α_2 , which muxed the output of the slicer, are sufficiently settled within 1UI. As a result, the proposed DFE is implemented two summers in four interleaves.

3. Circuit Implementation

3.1 Summer

Fig. 5 shows a summer with multiplexer implementation in even path. There are five input pairs as IN, S0, S180, IIR[1], and IIR[2], respectively. IN is the output of the CTLE as the input of the summer. The FIR tap is implemented with multiplexer and output of the slicer (S0 and S180 are utilized in even path summer, S90 and S270 are utilized in odd path summer). Finally, IIR[1:2] are the output of the IIR1/MUX and IIR2/MUX, respectively. The proposed summer with multiplexer is

Fig. 6 Schematic of slicer

Fig. 7 Schematic of IIR filter

the CML circuit, and the coefficient of each tap is adjusted externally. In the proposed summer, the multiplexer is implemented by stacking the transistor at the first post-cursor tap. Therefore, the FIR tap of two phases is implemented in one summer.

3.2 Slicer

The slicer that operates at CLK0 out of 4-phase is shown in Fig. 6. The slicer has three major design points. First, the transmission gate is implemented to maintain the input of the slicer because the summer operates in full-rate. Second, connect cross-coupled capacitors to the input and output of the slicer to eliminate the kickback effect that occurs when the signal of a large swing is coupled to the input node through the gate-to-drain capacitor [28]. Finally, charge-steering logic (CSL) circuit is utilized instead of CML circuit to enhance the power efficiency [29]. The CSL slicer consumes power when CLK0 is high, and the slicer is reset when CLK0 is low. So, the CSL slicer achieves high power efficiency.

3.3 IIR filter

The FIR filter removes one discontinuous post-cursor. The multi-tap FIR DFE that requires more slicers or d flip-flops to remove the long-tail ISI. So, the multi-tap FIR DFE consumes a lot of power. The IIR filter that removes multiple post-cursors consumes less power compared to the FIR filter [30, 31]. Fig. 7 illustrates the adjustable IIR filter. The IIR filter operates in full-rate and adjusts long-tail depending on the time constant. The

Fig. 8 Layout of the proposed DFE

Fig. 9 Simulated (a) channel frequency response (b) eye-diagram before equalization

Fig. 10 Simulated eye-diagram after the CTLE (a) minimum boosting (b) maximum boosting

time constant is determined by R and C. The IIR filter effectively eliminates long-tail ISI by adjusting C value. Then, the IIR filter is controlled by multiplexer implemented by stacking the transistors. So, the IIR filter that replaces the multiple discrete taps reduces power consumption.

4. Simulation Results

The proposed DFE is designed with 65-nm technology and tested in pre-layout simulations. The proposed DFE is verified by slow-slow (SS) corner 40°, the worst case, with 1.2V supply voltage using a spectre. Fig. 8. shows the layout of the proposed DFE excluding the CTLE. The proposed DFE occupies 0.023mm². The simulation result of channel frequency response is shown in Fig. 9(a). Fig. 9(b) depicts eye-diagram after channel with 21-dB loss at 14GHz. The eye is completely closed. Fig. 10(a) and Fig. 10(b) illustrate the eye-diagram after the CTLE with minimum boosting and maximum boosting,

Fig. 11 Simulated typical quad-rate DFE eye-diagram after CTLE maximum boosting

Fig. 12 Simulated proposed 1-FIR 2-IIR DFE with summer reduction technique eye-diagram after CTLE (a) maximum boosting (b) minimum boosting

respectively. The eye-opening after the CTLE with minimum boosting is achieved 0.26 UI. In maximum boosting, eye-opening is achieved 0.58 UI.

The simulation results of a typical quad-rate DFE are shown in Fig. 11. A typical quad-rate DFE is simulated with maximum boosting of the CTLE. A typical quad-rate DFE has four summers. So, the output of each summer is sampled by CLK0, CLK90, CLK180 and CLK270, respectively. The eye-opening of a typical quad-rate DFE is achieved 0.69 UI. The power efficiency of a typical quad-rate DFE is 1.32-pJ/bit.

Fig. 12 depicts simulation results of the proposed 1-FIR

Table I Power comparison of a typical DFE and the proposed DFE

	Typical quad-rate DFE	Proposed DFE
Supply voltage (V)	1.2	1.2
Data rate (Gb/s)	28	28
Number of summers	4	2
Summer power consumption (mW)	21.14	12.38
Total power (mW)	37.12	24.8
Power efficiency (pJ/bit)	1.32	0.88

Table II Performance comparisons

	[14]	[19]	[26]	[30]	This work
Process (nm)	130	28 (LP)	45 SOI	28 FDSOI	65 GP
Data rate (Gb/s)	4.5	10	12	16	28
Max loss (dB)	22	24	15	28	21
Supply (V)	1.2	1	1	1	1.2
DFE Power (mW)	12.4	4.1	11	15.8	24.8
Area (mm ²)	0.14	0.008	0.003	0.008	0.023
Power efficiency (pJ/bit)	2.8	0.41	0.92	0.99	0.88

2-IIR DFE with summer reduction technique. In Fig. 12(a), the proposed DFE achieved 0.69 UI eye-opening with maximum boosting of the CTLE. The power efficiency of the proposed DFE is 0.88-pJ/bit. So, the proposed DFE reduces power consumption by 33% compared to a typical quad-rate DFE while maintaining performance. Also, the simulation results of the proposed DFE with minimum boosting of the CTLE are shown in Fig. 12(b). The proposed DFE achieved 0.59 UI eye-opening. Consequently, the proposed DFE complements all ranges of CTLE. Table I shows the power comparison between a typical quad-rate DFE and the proposed DFE. A typical quad-rate DFE has four summers and the proposed DFE has two summers, and the rest of the conditions are the same. A typical quad-rate DFE summer consumes 21.14mW. The proposed DFE dissipates 12.38mW. So, the proposed DFE with summer reduction technique reduces total power by 33%. Table II illustrates a summary of performance compared to previous work. The DFE power consumption consists of dynamic power and the area represents the core circuit. Among the compared previous work, the proposed DFE has better performance in power consumption and active area.

5. Conclusions

The quad-rate 1-FIR 2-IIR DFE with summer reduction

technique is proposed in 65nm CMOS technology for high-speed wireline communication. The proposed DFE halves the number of summers by using resetable slicer and summer with multiplexer. Also, the proposed DFE further reduces power by using a quad-rate structure and IIR filters. The proposed DFE reduces power consumption by 33% compared to a typical quad-rate DFE. The maximum eye-opening of the proposed DFE is 0.69 UI, and power efficiency is 0.88-pJ/bit at 28Gb/s.

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