Design of broadband high-gain GaN MMIC power amplifier based on reactive/resistive matching and feedback technique

Lin Peng¹, Jianqiang Chen¹, Zhihao Zhang¹(✉), Yang Huang², Tong Wang², and Gary Zhang¹

Abstract This paper presents a K-band two-stage power amplifier (PA) with a compact circuit size of 1.8×0.87 mm². To guarantee broadband high-gain output performance, the optimal impedance domain and power cell are determined through load/source-pull simulation and K-point method, respectively. Reactive/resistive matching networks are carefully employed to reduce the equivalent gate capacitance, improve stability and compensate for the device’s negative gain roll-off slope. Meanwhile, combining with feedback technique adopted in driver stage, the entire operation bandwidth can be further extended. Under 12 V pulse voltage supply, 37.4% of peak power-added efficiency (PAE) at 26 GHz and 24±0.5 dB of small-signal gain, 30.3–31.6 dBm of saturated output power ($P_{\text{sat}}$) across 22–27 GHz are obtained as shown in the experimental results.

Keywords: gallium nitride (GaN), monolithic microwave integrated circuit (MMIC), broadband power amplifier, feedback

Classification: Microwave and millimeter-wave devices, circuits, and hardware

1. Introduction

The extensive application and rapid development of wireless technology have led to the derivation of many types of communication systems. They usually adopt diverse standards or work in separated frequency ranges, resulting in mutual independence and thus requiring additional equipment for interconnection, which would increase costs and affect the operation reliability when close collaboration between distinct systems is necessary. In such context, broadband communication systems came into being and have been widely applied in modern commercial and military fields to date [1, 2, 3]. Besides, with the arrival of the 5G era, large bandwidth is also the essential ingredient to satisfy ever-growing mobile traffic volume demand [4, 5]. Therefore, broadband PAs are attracting more attention and gradually become the focus of research.

Due to the gain roll-off characteristics of transistor and its input and output impedances vary with frequency, how to achieve small-scale fully integrated 1-Watt PA with more than 20% fractional bandwidth and over 22 dB small-signal gain is the major issue to be solved in this study. Discussing the current mainstream of several typical broadband configurations, distributed amplifier has the widest bandwidth by incorporating the parasitic capacitances of multiple cells in parallel into artificial transmission lines, but it generally suffers from low gain, limited power level, and bad integration [1, 6, 7, 8]. Although the balanced amplifier is capable of reaching one-octave bandwidth, it requires bulky 3 dB couplers and large power consumption [5, 9, 10, 11]. The reactive/resistive topology can provide a positive roll-off insertion loss slope for gain compensation, but its modest bandwidth and relatively poor VSWR are the main drawbacks [12, 13]. Another commonly used broadband amplification structure is negative feedback [2, 14, 15, 16], which offers obvious advantages in terms of cost, space, and complexity. However, the introduction of a feedback resistor brings the problem of gain degradation that needs to be tackled by the active device with large transconductance. In this regard, GaN, the third-generation wide-bandgap semiconductor technology, with superior breakdown voltage and electron mobility properties is the promising candidate. Moreover, GaN-based devices also have the inherent benefit of high output resistance along with low parasitic capacitance, which makes them ideal for broadband amplifier design [1, 17, 18]. Accordingly, we propose a solution that combines reactive/resistive gain equalizing networks in the form of parallel RC and negative feedback technique to realize a cascaded two-stage MMIC PA covering 22–27 GHz based on 0.1 µm GaN high electron mobility transistor (HEMT) process on a 100-µm-thick silicon substrate developed by OMMIC.

2. Analysis and design of broadband PA

2.1 Unit cell selection

Concerning the requirements of miniaturization and good PAE, it’s preferable to adopt two-stage common-source architecture for PA. In doing so, there may be a risk of...
insufficient gain owing to the inevitable loss of matching networks (MNs) and the maximum available gain (MAG) of a single transistor. In consequence, the total gate width (TGW) of power stage cell should be selected as small as possible under the premise of meeting 1 W $P_{sat}$ and is calculated to be 370 μm when given 1 dBm trade-off margin with a moderate power density of 3.4 W/mm. Higher optimal impedance can be obtained concurrently, which helps simplify matching. Note, TGW is the product of unit gate width (UGW) and the number of gate fingers (NGF), which impacts the device’s gain transition from maximum stable gain (MSG) into MAG. Since the turning frequency point involved is exactly where the Rollett’s stability factor K becomes unity, we call it K-point, which is better to fall outside the upper band boundary to ensure that the active device has enough intrinsic gain [19]. The simulated dependence of the K-point on TGW of three kinds of unit cells is depicted in Fig. 1, from which we can conclude that using devices with larger TGW is less suitable for higher frequencies due to the falling K-point.

On the other hand, when the gate periphery is set, as the NGF increases by a multiple of 2 for the sake of layout symmetry, there is an increasing phase difference between gate fingers and the middle sources of transistor have a long electrical path to via-hole ground, extra parasitic inductance will be generated, leading to a reduction in forward gain. Yet at the same time, the decrease of UGW helps to avoid excessive phase errors as well as signal propagation fade along the gate, then the most amount of gain can be preserved [20]. Taking into account these factors, Fig. 1 reveals that minor UGW is the dominant contributor to a higher K-point for the same TGW. According to device scaling rules of UGW≤100 μm and NGF≤8 recommended by the foundry design manual in conjunction with TGW of 370 μm, the corresponding three transistors and their K-point information are summarized in Table I. Among them, the 8-finger FET cell was chosen for output stage, a 46×4 μm cell was thereafter assigned in prior stage to deliver adequate linear power depending on a conservative staging ratio of 1:2 on account of soft compression phenomena of GaN-based devices. It is worth mentioning that each cell was biased at equal –1 V $V_{gs}$ to yield maximum transconductance and thus elevated power gain as suggested in Fig. 2.

![Fig. 1. Simulation of the dependence of the K-point on TGW.](image)

<table>
<thead>
<tr>
<th>NGF</th>
<th>UGW (um)</th>
<th>K-point (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>92</td>
<td>20.7</td>
</tr>
<tr>
<td>6</td>
<td>62</td>
<td>25.4</td>
</tr>
<tr>
<td>8</td>
<td>46</td>
<td>28.4</td>
</tr>
</tbody>
</table>

Table 1. K-points corresponding to different fingers of unit cells with equal TGW.

![Fig. 2. Simulated DC/AC transconductance $g_m$ for a 46×8 μm HEMT at $V_{ds}=12$ V.](image)

2.2 Parallel RC gain equalizing network design

To flatten the gain response inside the specified bandwidth, we employed a parallel RC gain equalizing network placed in the input terminal of transistor, which also has the function of improving stability and reducing parasitic effects, primarily the gate-source capacitance $C_{gs}$. To strike a balance between these three aspects while maintaining reasonable MAG, the simplified small-signal equivalent circuit of a GaN HEMT is first given in Fig. 3 including seven intrinsic frequency-dependent elements which can be analytically extracted through Y-parameters obtained from S-parameter simulation of nonlinear FET model for a certain bias point [21].

![Fig. 3. Equivalent circuit model of a GaN HEMT.](image)
Based on Fig.3 and Eq. (1), channel resistance $R_i$, depletion capacitance $C_{gs}$ and $C_{gd}$ can be expressed as

$$R_i = \text{Re} \left( \frac{1}{y_{11} + y_{12}} \right) \quad (2)$$

$$C_{gs} = \left[ -\omega \text{Im} \left( \frac{1}{y_{11} + y_{12}} \right) \right]^{-1} \quad (3)$$

$$C_{gd} = \frac{1}{\omega} \text{Im} \left( -y_{12} \right) \quad (4)$$

Using Eq. (2) to (4), $R_i = 5.3 \, \Omega$, $C_{gs} = 0.655 \, \text{pF}$, and $C_{gd} = 0.087 \, \text{pF}$ for a 46×8 μm HEMT are derived at 27 GHz under 12 V supply. Because $C_{gd}$ is rather smaller than $C_{gs}$, the cell is treated as a unilateral two-port network for simplicity, and the input impedance $Z_{in}$ seen from the gate node of transistor is therefore modeled by means of a series connection of $R_i$ and $C_{gs}$.

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**2.3 Analysis and design of the feedback loop**

A lossy feedback network from the drain to the gate of the device is another effective way in controlling gain ripple, amplifier stability, and matching which also contributes to making the circuit insensitive to ambient temperature and process variation [24, 25], bringing a significant improvement in robustness. So a feedback loop composed of L-R-C in series is introduced connected to the 46×4 μm cell, as illustrated in Fig. 6.

$$[Y]_{f} = \left[ \begin{array}{cc} y_{11} & y_{12} \\ y_{21} & y_{22} \end{array} \right] = [Y]_{\text{HEMT}} + [Y]_{f}$$

$$S_{21} = \frac{-2Y_{0}y_{12}}{(Y_{0} + y_{11})(Y_{0} + y_{12}) - y_{12}y_{21}}$$

In order to lower the equivalent gate capacitance so as to ease interstage matching, the value of $C_p$ in parallel RC network presented in Fig. 4 should be less than $C_{gs}$, while the thin-film resistor $R_p$ is responsible to absorb low-frequency gain and reduce negative resistance that appears at device gate [1]. Nevertheless, $C_p$ could not be too small, otherwise the wanted signal will be greatly attenuated by $R_p$. For this reason, putting identical emphasis on bypassing the in-band RF component is necessary, thereby we take $\text{MAG} > 10 \, \text{dB}$ at the upper edge of the operation band as another constraint for $C_p$ selection and with the adjustment of $R_p$ together to facilitate uniform gain at the expense of acceptable loss. Finally, $C_p$ and $R_p$ were respectively determined to be 0.47 pF and 25 Ω in a compromise. The gate bias branch formed by 50 Ω resistor $R_s$ and choke spiral inductor in series mainly aims to further eliminate potential spurious oscillations and prevent the leakage of RF energy [22, 23], whereas it has negligible effect on the amplification chain within the band of interest. Fig. 5 plots detailed comparisons of the foresaid stabilization measures.
Recall the expression of transducer gain, we have [12]

\[
G_T = \frac{|S_{21}|^2 (1-|\Gamma_s|^2)(1-|\Gamma_L|^2)}{|(1-S_1G_s)(1-S_{22}G_L)-S_{12}S_{22}G_sG_L|^2}\]  (9)

If both the source and load are matched to characteristic impedance \(Z_0\), the reflection coefficient \(\Gamma_s=\Gamma_L=0\) and \(G_T\) simply becomes \(|S_{21}|^2\). From Eq. (5) to (9), the desired gain response and stability enhancement can be achieved by properly tuning the feedback components. In design, 0.5 nH inductor was added for the purpose of reducing the effectiveness of negative feedback with increasing frequency, while the 0.41 pF capacitor not only serves as a DC block to keep the isolation between the gate and drain bias but also regulates the phase and magnitude of feedback waveform. Next, 57 Ω resistor was selected to raise the valley K-factor within 10–30 GHz to slightly below 1 without sacrificing too much gain and smooth the frequency response. In addition, care must be taken to check that there are no frequencies where the feedback could cause a regenerative unstable condition.

### 2.4 Design strategy for matching networks

The output capability of PA depends to a large extent on output MN, we started by determining the optimal complex impedance domain in the range of 22–28 GHz to ensure that PA’s performance at 27 GHz still fully meets the specifications even in the worst case. Iterative load/source-pull procedures of the stabilized GaN HEMT with an input power about \(P_{1dB}\) were carried out at low, medium, and high fundamental frequency points, whereas the influence of harmonics was ignored as they locate away from the passband and can be easily filtered out [3, 27, 28].

![Optimal load impedance of fundamental](image)

From Fig. 7, it is clearly observed that the contour for load impedances whose inside fulfill the set goal of either \(P_{1dB}>31\) dBm or \(\text{PAE}>40\%\) is constantly getting narrower and moving in a counter-clockwise direction towards the real axis of the Smith Chart attributed to the strengthening innate output parasitics as frequency increases, which explains the tolerance region defined by the overlapping portion of three groups of contours is mostly restricted by the contours at 28 GHz. That means broadband matching tends to match at high-frequency side, wider bandwidth can be produced through appropriately modifying the degree of mismatch at low frequencies. Subsequently, \(Z_{L,\text{opt}}=12+j*14.6\ \Omega\) and \(Z_{S,\text{opt}}=4.5+j*11.2\ \Omega\) were selected as the initial targeted center values. The output MN transforms 50 Ω to \(Z_{L,\text{opt}}\) with series microstrip lines and shunt low capacitance density capacitors instead of open-circuited stubs for shrinking the occupation area, and plays a vital role in suppressing harmonic distortion, while the interstage MN was synthesized to conjugetly match two devices for maximum gain. As regards input MN, is intended to improve the terminal return loss. After cascading all independently designed MNs with two transistors in order, the stagger-tuning technique was undertaken to realize the mutual compensation of the insertion loss of MNs in different frequency ranges with the consideration of microstrip discontinuities, cross-coupling, and actual wedge-bonding wires, broadband gain response can be achieved eventually. In particular, the drain feed traces used double-layer metal with a total thickness of 2.5 μm to handle high current swing. At last, we conducted a thorough nonlinear EM co-simulation of the complete layout shown in Fig. 8 to verify the amplifier was unconditionally stable under any possible levels of incident power throughout the whole band.

![Micrograph of the proposed PA](image)

### 3. Fabrication and measurement results

Fig. 9 is the photo of a bare-die chip mounted to the test fixture. Gate bias voltage was adjusted to reach the same quiescent current draw of 170 mA as in simulation under 12 V supply in pulse mode with 5% duty-cycle and 1 ms duration to avoid overheating during continuous tests. Small-signal results in Fig. 10 exhibit that the fabricated PA features 24±0.5 dB linear gain over 22–27 GHz, and the input and output reflection coefficients are less than −9.2 dB and −11.3 dB, respectively. Compared with the simulated one, measured \(S_{21}\) has a low-frequency offset of approximately 0.8 GHz and is overall higher, but the trends of the two curves are basically consistent.
In the same band and at room temperature, Fig. 11 and Fig. 12 indicate that $P_{\text{4dB}}$ exceeds 28.3 dBm, $P_{\text{sat}}$ fluctuates between 30.3–31.6 dBm, the PAE at $P_{\text{sat}}$ reaches 30.5%–36.9%. Notably, the best performance of designed PA occurs at 26 GHz, corresponding power sweep characteristic curve is plotted in Fig. 13, where the peak PAE approaches 37.4% found around $P_{\text{6dB}}$ at an input power of 14 dBm. Table II lists the performance comparison of some related PAs.

### Table II. Comparison with previous studies.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Freq (GHz)</th>
<th>FBW (%)</th>
<th>Gain (dB)</th>
<th>$P_{\text{out}}$ (dBm)</th>
<th>PAE (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[9]</td>
<td>32–38</td>
<td>17.1</td>
<td>17±0.5</td>
<td>36.2–37.2</td>
<td>25–34</td>
</tr>
<tr>
<td>[17]</td>
<td>29–34</td>
<td>15.9</td>
<td>23±1</td>
<td>37.5–39.8</td>
<td>30–35.5</td>
</tr>
<tr>
<td>[29]</td>
<td>25–29</td>
<td>14.8</td>
<td>22.7±0.7</td>
<td>25.6–26.3</td>
<td>27.2–32.5</td>
</tr>
<tr>
<td>[30]</td>
<td>19–23</td>
<td>19.1</td>
<td>23.6±1.4</td>
<td>35.1–37.3</td>
<td>20–29.8</td>
</tr>
<tr>
<td>This work</td>
<td>22–27</td>
<td>20.4</td>
<td>24±0.5</td>
<td>30.3–31.6</td>
<td>30.5–36.9</td>
</tr>
</tbody>
</table>

### 4. Conclusion

A two-stage broadband PA operating in 22–27 GHz band is demonstrated and fabricated in a 0.1 μm GaN HEMT process. To obtain high gain, the optimum device geometry is evaluated based on K-point method to derive a perfect combination of NGF and UGW after specifying the right TGW. Parallel RC gain equalizing networks and feedback technique are both utilized to get gain flatness and enhance stability simultaneously. The concept of optimal impedance domain is applied in the design to achieve broadband output performance. With the help of multistage matching networks, the transistor’s gain rolloff characteristics can be further compensated while accomplishing low-Q impedance transformation. The 1.57 mm² MMIC chip exhibits a measured small-signal gain of 24 dB averagely with 0.5 dB variation across 22–
27 GHz and delivers more than 30 dBm $P_{sat}$ associated with 30.5%–36.9% of PAE which match the simulation expectations with a nice agreement. Measurement results prove that the proposed compact broadband PA fits the practical K-band transmitter systems.

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References


