LETTER

Analysis of Novel Phase-Shifted Full-Bridge Converters with Wide ZVS range Reduced Filter Requirement

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Abstract In this paper, some novel converters are proposed to solve the drawbacks of traditional phase-shifted full-bridge (PSFB) converter. In the primary side of proposed converters, the FB inverter is divided into two half-bridge inverters and the large-sized transformer is replaced by two small-sized transformers. By employing this structure, the zero voltage switching range can be extended and the primary circulating current existing in the additional PSFB converter is removed. In the secondary side, various rectifiers can be adopted to suit for different applications. Moreover, the primary power can be continuously transferred to secondary side in the proposed converters, which contributes to the reduction of output filter requirement. The circuit configuration, operational principle and relevant analysis of proposed converters are introduced in this paper. Experimental results on two typical prototype converters are built to validate the theoretical analysis.

key words: full-bridge converter, zero voltage switching (ZVS), circulating current, filter requirement

Classification: Power devices and circuits

1. Introduction

The phase-shifted full-bridge (PSFB) converter is the most widely adopted topology for high-power isolated DC-DC power conversion due to its simplicity and efficiency [1-6]. In the primary side of PSFB converter, four switches are controlled with phase-shifted modulation method, which makes it possible to achieve zero-voltage switching (ZVS) without the help of any auxiliary circuits [7-10]. The secondary structure consists of a rectifier and LC filter. Generally, the loss of rectifier is the main contributor to the total power loss of PSFB converter. Thus, different rectifier such as full-bridge rectifier (FBR) [11-13], center-tapped rectifier (CTR) [14-16] and current doubler rectifier (CDR) [17-20] can be applied to suit for various applications. In the FBR structure, there are only two secondary winding, which leads to lower transformer volt-ampere requirement and voltage stress but it takes high conduction loss. As for

the CTR structure, during the transfer of power, only one diode conducts so it can take less conduction loss. However, the structure of transformer is complex and the voltage stress of diode is high. The winding structure of the CDR is simple and has few diodes at the same time, so it is preferred to be used in low-voltage high-current applications.

However, the traditional PSFB converter has some serious problems such as narrow ZVS range and primary circulating current. At light loads, the lagging switches lose ZVS and the conversion efficiency is severely degraded. In addition, the primary voltage is zero but the primary current is non-zero and this current just circulates in the primary side without transferring any power to the secondary side during the freewheeling interval. It causes excessive conduction loss and increased output filter requirement.

In order to solve the aforementioned problems and improve the performance of PSFB converter, many novel FB converters have been researched in the literature. The ZVS range can be extended by increasing the leakage inductance of main transformer. However, this method results in high duty-cycle loss and primary conduction loss. In [21-23], some novel PSFB converters with auxiliary circuits are proposed. The ZVS energy is independent of load current in these converters. Thus, primary switches can achieve ZVS under all operating conditions. But the primary circulating current still exists. It can be significantly reduced by utilizing the technology of zero-voltage and zero-current switching (ZVZCS) [24-26]. The primary current is reset by the introduced auxiliary circuits and it is maintained at zero during the freewheeling interval. The output power is maintained constant by the energy stored in the output filter, thus large filter requirement is required in these ZVZCS converters.

Recently, the PSFB converters with dual transformer are very attractive due to their outstanding performance [27-31]. Fig.1 shows two typical converters with FBR [28] and CTR [29]. As shown in Fig.1, the FB inverter is divided into a leading half-bridge (HB) and a lagging HB in the primary side. Compared to the traditional PSFB converters, these converters can achieve the following advantages: (1) All switches can achieve ZVS operation

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under entire load conditions; (2) The conduction loss is greatly improved since the circulating current is fully eliminated in the proposed converter; (3) The primary power can be continually transferred to the secondary side, so the requirement of output filter is significantly reduced.

Fig. 1 Typical converters with (a) FBR [28] and (b) CTR [29].

Fig. 2 Proposed converters with different rectifiers: (a) Converter #1; (b) Converter #2; (c) Converter #3; (d) Converter #4.

In order to enrich the family of PSFB converters with dual transformer, this paper proposes some novel typologies, as shown in Fig.2. In these converters, the primary structure is fixed but various rectifiers can be adopted in the secondary side. Fig.2(a) and Fig.2(b) show the converters with different CDR. The hybrid rectifier (Hyb-R) is composed of a CTR section and a FBR section. It is adopted in Fig.2(c) and Fig.2(d). These typologies allow the proposed converters to have the advantages of wide ZVS range and reduced filter requirement. This paper is organized as follows. As an example, the operational principle of proposed converter

with CDR is presented in Section II. The relevant analysis and experimental results are described in Section III and Section IV, respectively. Finally, Section V concludes this paper.

2. Operational Principle

One of the proposed converters, as shown in Fig.2(a) is taken as an example to verify the feasibility. In order to illustrate the operation principle, several assumptions are made as follows: (1) the blocking capacitor C_B and the output inductors L_1 & L_2 are large enough to be considered as constant voltage source of $0.5V_{in}$ and current source of $0.5I_o$, respectively; (2) the primary switches are ideal MOSFETs with body diodes and parasitic capacitors; (3) the leakage inductances of T_1 and T_2 are L_{k1} and L_{k2} , respectively; (4) the magnetizing inductance of the T_2 is L_m .

Fig.3 shows the simplified equivalent circuit with current and voltage notations. The phase-shifted control method is employed in the proposed converter. The key operational waveform can be obviously acquired by using PSIM software. Based on the simulation results, the key waveforms of Converter #1 can be shown in Fig.4. In the analysis, T_α indicates the shifted time between the leading-leg and the lagging-leg. On account of the symmetric structure of the converter, only the first half cycle is detailed in this article and the corresponding equivalent circuits are shown in Fig.5. The operating states can be divided into the following parts.

Fig. 3 Equivalent circuit with current and voltage notations.

Fig. 4 Key waveforms of Converter #1

State 1 [$t_0 \sim t_1$]: When switches Q_1 and Q_4 are in ON-state and diodes D_2 and D_3 are conducting, the primary voltages of T_1 and T_2 are $0.5V_{in}$. The rectified voltages $v_{r1}(t)$ and $v_{r2}(t)$ are $0.5nV_{in}$ and nV_{in} , respectively.

State 2 [$t_1 \sim t_2$]: When switch Q_1 turns off at t_1 , the leading-leg current starts to charge the capacitance of Q_1 and to discharge the capacitance of Q_3 . In this state, the leading-leg voltage and the secondary voltage of T_1 linearly decrease. The diode D_2 conducts naturally when the secondary voltage of T_1 falls to zero at t_2 .

State 3 [$t_2 \sim t_3$]: Since the secondary voltage of T_1 is clamped to zero by D_1 and D_2 at t_2 , the resonance of the leakage inductances of T_1 and the junction capacitors of T_1 and T_2 occurs in the leading-leg, which results in the sinusoidal deduction of the leading-leg voltage.

State 4 [$t_3 \sim t_4$]: When the leading-leg voltage falls to zero at t_3 , the parasitic diode of Q_3 begins to conduct and the ZVS turned-on of Q_3 naturally. In this state, the current of the D_1 increases and the current of the D_2 decreases.

State 5 [$t_4 \sim t_5$]: This state begins when the current of the D_2 and the leading-leg current fall to zero at t_4 . In this state, the primary power is transferred to the secondary side only through the lagging transformer. The primary and secondary voltages of T_2 are $0.5V_{in}$ and $0.5nV_{in}$, respectively.

State 6 [$t_5 \sim t_6$]: When Q_4 turns OFF and $i_m(t)$ reaches to the maximum value at t_5 , D_4 starts to conduct and the resonance of leakage inductances and junction capacitors occurs in the primary side. The communication between D_3 and D_4 is progressed, the current of D_4 increases and the current of D_3 decreases. This state ends when the lagging-leg voltage $v_{lag}(t)$ reaches to V_{in} .

Fig. 5 Equivalent circuits: (a) State 1 [$t_0 \sim t_1$]; (b) State 2 [$t_1 \sim t_2$]; (c) State 3 [$t_2 \sim t_3$]; (d) State 4 [$t_3 \sim t_4$]; (e) State 5 [$t_4 \sim t_5$]; (f) State 6 [$t_5 \sim t_6$]; (g) State 7 [$t_6 \sim t_7$].

State 7 [$t_6 \sim t_7$]: In this state, $v_{lag}(t)$ reaches to V_{in} , and the voltage across Q_2 falls to zero, which provides favorable conditions to the ZVS of the Q_2 . The currents of leading-leg and lagging-leg rise in the negative direction because of the existence of voltage across leakage inductances. Besides, the communication between D_3 and D_4 is continually progressed in the secondary side. When $i_{D3}(t)$ falls to zero, this state ends up and D_3 is naturally turned OFF. The input power transferred from the T_1 and T_2 simultaneously to the secondary side.

On account of the symmetric structure of the converter, the next half cycle (State 8 to State 14) are the same as previous states except for the direction of powering path.

3. Relevant Analysis

3.1 Voltage Gain

Since the switches are controlled with phase-shifted modulation, the voltage gain depends on the shifted time in the proposed converter. The duration of ZVS transitions are so narrow that only the intervals of State 1, State 5 and State 8, State 12 should be considered and the other states can be ignored. Fig.6 shows the simplified waveforms of rectifier voltages. As shown in Fig.6, the rectified voltage in the proposed converter #1 is a three-level waveform, and the traditional PSFB with CDR is only a two-level waveform. During the duty-cycle interval, the rectified voltage is nV_{in} and the output voltage can be regarded numerically as the average of the rectifier voltage. According to calculation, the voltage gain of the proposed converter #1 is $0.5D+0.25$, higher than the voltage gain of the traditional PSFB with CDR. The efficiency will be effectively improved because it is obviously that the high-voltage conversion ratio will not only cut down the secondary-turns number of transformer, but decrease voltage stress of rectified diodes.

Fig. 6 Simplified waveforms of rectifier voltages (a) in the proposed converter, (b) in the traditional PSFB converter with CDR.

3.2 ZVS conditions

From the operational principle of the proposed converter #1, the ZVS transition can be divided into the condition of the leading-leg switches and the lagging-leg switches. Firstly, in the leading-leg switches, the ZVS progress can be separated into two parts, State 2 and State 3. In the State 2, the leading-leg current can be regarded as a constant current source and its value is nI_o .

As a result of the leading-leg, the voltage $v_{lea}(t)$ decreases in a linear way firstly, and $v_{lea}(t)$ decreases with a sinusoidal waveform to zero because of the resonance between leakage inductance and junction capacitors. Therefore, at t_3 , $v_{lea}(t)$ falls to zero, and the switches can achieve ZVS. Since the remaining energy in the junction capacitors accounts for a quarter of the total energy, the leading-leg switches can implement a wide ZVS range in a easier way. Besides, from the analysis of the lagging-leg switches, not only the leakage inductances react on the ZVS transition of lagging-leg, but also they play an important role in the process. When adopting a large magnetizing current, the ZVS range can be extended without sacrificing the primary conduction losses, which different from the obvious conduction loss of all primary components in the traditional converter. At the same time, the lagging-leg switches can use the low-current-rated MOSFETs with small junction capacitors, which is helpful to achieve wider ZVS range and the lower primary conduction losses.

3.3 Voltage stress of rectified diodes

For the voltage stress calculation of rectified diodes, the secondary voltage oscillation generated by parasitic circuit element is ignored to simplify the calculation. It is shown that the voltage stress of D_1 , D_2 and D_3 , D_4 in the proposed converter #1 are $0.5nV_{in}$ and nV_{in} , respectively. The above analysis indicates that the voltage stress of the proposed converter #1 is very low. Thus, the low-voltage-rated diodes can be employed in the topological structure to reduce the power loss and improve the system performance.

3.4 Performance Comparison

To help tradeoff design and topology selection in engineering applications, Table I shows the performance comparison among different converters. The proposed converter #1 and the proposed converter #3 have the least numbers of secondary components, thus they are more practical for applications. The proposed converters #1,#2 and #4 employ CDR in the secondary side, and they are well suited for the applications with high output current. For the converters with FBR, the voltage stress of rectified diodes is the smallest and they can be adopted in high output voltage applications. On the contrary, the voltage stress of diodes in the CTR converters is the highest and these converters are preferred to be used in low-voltage applications. As shown in Fig.2, the Hyb-R is composed of a FBR section and a CTR section. As a combined topology, the voltage stress of diodes in the Hyb-R converters is between that of FBR and CTR, which makes them well appropriate for the applications with medium output voltage.

Table 1 Performance comparison among different converters.

Converter	#1	#2	#3	#4	FBR	CTR
N^*	7+2W	9+4W	6+3W	7+3W	8+2W	6+4W
Voltage gain	$\frac{D}{2} \frac{1}{4}$	$\frac{D}{2} \frac{1}{4}$	$\frac{D}{2} \frac{1}{2}$	$\frac{D}{2} \frac{1}{4}$	$\frac{D}{2} \frac{1}{2}$	$\frac{D}{2} \frac{1}{2}$
Stress of diode	nV_{in}	nV_{in}	$1.5nV_{in}$	$1.5nV_{in}$	nV_{in}	$2nV_{in}$
Output voltage	High	Low	Medium	Medium	High	Low
Output current	High	High	Medium	High	Low	High

N^* means number of secondary components, nW means number of secondary windings.

4. Experimental result

Two experimental prototypes based on Fig.2(a) converter #1 and Fig.2(c) converter #3 are built to verify the theory analysis since the circuit structures are simple and they are relatively easy to implement. These two prototypes have the same specifications, as follows: input voltage 320~400V; output voltage 120V; maximum output power 1200 W; switching frequency 100 kHz.

Fig.7 and Fig.8 show the key waveforms of transformers in the proposed converters #1 and #3, respectively. As shown in Fig.7(a) and Fig.8(a), the primary current of T_1 i_{p1} falls to zero when the ZVS transition of leading switches finish. On the other hand, the primary voltage of T_2 V_{p2} is in phase with the primary current i_{p2} . There is no circulating current in the proposed converters. The primary energy is continuously transferred to the secondary side through T_2 during the whole switching period. This feature contributes to reducing the output filter requirement. The experimental results demonstrate the theoretical analysis pretty well.

Fig.9 and Fig.10 show the ZVS waveforms of leading-leg and lagging-leg switches at light load. As seen, all the switches are successfully turned on with ZVS. Therefore, a wide ZVS range can be achieved in the proposed converters.

Fig. 7 Key waveforms of transformers in converter #1, (a) T_1 ; (b) T_2

Fig. 8 Key waveforms of transformers in converter #3, (a) T₁; (b) T₂

Fig. 9 ZVS waveforms at light load $I_o = 2$ A in the converter #1 (a) Leading-leg switch; (b) Lagging-leg switch.

Fig. 10 ZVS waveforms at light load $I_o = 2$ A in the converter #3 (a) Leading-leg switch; (b) Lagging-leg switch.

5. Conclusion

In this paper, some novel converters with two transformers are proposed to overcome the disadvantages of traditional PSFB converter such as narrow ZVS range and large output filter requirement. The distinctive characteristics of proposed converters are summarized as follows:

- (1) All switches achieve ZVS operation along wide load ranges.
- (2) The primary power can be continuously transferred to the secondary side, which contributes to the reduction of output filter requirement.
- (3) Various rectifiers can be adopted to suit for different applications.

The theory analysis and performance are fully validated on hardware prototypes.

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