LETTER

A 2.2 ppm/°C compensated bandgap voltage reference with a double-ended current trimming technique

Wenxin Yu¹, Lenian He², Jianxiang Xi³, Quan Sun⁴, and Changyou Men⁵

Abstract This paper presents a high-precision bandgap voltage reference (BGR) with a double-ended current trimming technique. A high-order curvature compensation method is adopted to compensate for the nonlinearity of $V_{BE}$. The proposed trimming technique using the one-time programmable (OTP) programming cancels the errors caused by process variation and enables bulk production, which achieves a best TC of 2.2 ppm/°C from -40°C to 125°C. The proposed BGR is fabricated in a 0.18-um BCD process with an active area of 0.329 mm². The line sensitivity is 0.18 %/V operating from 2.9 V to 3.6 V.

Key words: bandgap reference, temperature coefficient, current trimming, high-order curvature compensation

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

Bandgap voltage reference (BGR), which provides stable voltage or current, plays an indispensable role in mixed systems [1]. The increasing demand for modern high-performance circuits, such as analog-to-digital converters and voltage regulators, raises a need for high-precision, low temperature coefficient (TC) voltage reference.

The basic idea of BGR is to add a proportional to absolute temperature (PTAT) voltage to the emitter-base voltage ($V_{BE}$) of bipolar junction transistor (BJT) [2, 3], which compensates for the first-order linear term of $V_{BE}$. Due to its remaining nonlinear portion, it’s hard to reduce TC to less than 10 ppm/°C [4]. Therefore, several effective high-order curvature compensation techniques are proposed to solve the problem [5, 6, 7, 8, 9, 10, 11, 12]. Besides, there still exist other error sources that degrade the performance of BGR, such as base resistance spread, temperature dependence of current gain $\beta$, and opamp offsets. Chopping technique is used to cancel the opamp offset. The residual errors are mainly PTAT and can be removed by temperature trimming [13, 14, 15, 16, 17, 18]. Ref. [19] proposed a two-temperature trimming method based on a new base expansion, which achieves less than 1 ppm/°C simulation result. But this method needs one hot temperature, leading to a long time for measurement and trimming. Ref. [20] proposes a method of resistor trimming, dividing the resistor into several small resistors in series to adjust PTAT voltage. However, it is single-ended and it needs a complex control system to enter trim code. More importantly, due to process variation, the output voltages of different dies are discrete in the vertical direction, meaning they must be trimmed with these techniques.

This paper presents a BGR with a novel double-ended trimming technique. One-time programmable (OTP) with $1\degree$C control is adopted to enter an 8-bit trim code for reducing time and cost. This trimming technique can trim all dies in a wafer at once. Results show that the BGR achieves a low TC of 2.2 ppm/°C over -40 ~125 °C, and a line sensitivity of 0.18 %/V.

The paper is organized as follows. Section II describes the principles of the proposed BGR structure with high-order curvature compensation. The double-ended current trimming technique using OTP is introduced in Section III. Section IV presents the simulation and test results. The conclusions are included in Section V.

2. Proposed BGR structure with high-order compensation

The diagram of the proposed BGR is shown in Fig. 1, which consists of a high-order compensation, a BGR core, a class-AB output, and a current trimming. High-order compensation is used to compensate for the nonlinearity of $V_{BE}$. The current trimming technique is a-

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¹Institute of VLSI Design, Zhejiang University, Hangzhou 310058, China
²HangZhou Vango Technologies, Inc., Hangzhou 310052, China
a)helenian@zju.edu.cn

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applied to improve the accuracy of output voltage and achieve better TC. After testing the $V_{\text{OUT}}$ curve as a function of temperature, the trimming circuit works for adjusting the PTAT current generated in BGR core. Then it re-outputs $V_{\text{ref}}$ and $V_{\text{OUT}}$ as $V_{\text{ref,trim}}$ and $V_{\text{OUT,trim}}$. What’s more, the class-AB output increases the drive capacity of $V_{\text{OUT}}$ to provide heavy current [21].

2.1 Schematic of proposed BGR core
The schematic of the proposed BGR core is shown in Fig. 2, including common-mode feedback (CMFB) amplifier, $V_{\text{ref}}$ generation block, compensation block, and trimming block. CMFB circuit keeps $V_X$ and $V_Y$ equal to $V_{\text{ref}}$ to make the loop stable. $I_{\text{trim}}$ is the current produced by trimming block, which is injected into $V_X$ or $V_Y$. $V_{\text{ref}}$ generation block is used to generate bandgap reference $V_{\text{ref}}$. The current flows through $R_1$ can be written as:

$$I_c = (kT/qR_c)\ln n$$  \hspace{1cm} (1)

Where $k$ is the Boltzmann constant, $q$ is the electron charge, and $n$ is the ratio of $Q_2$ and $Q_1$. The value of $n$ is set to be 9. The reference voltage $V_{\text{ref}}$ can be written as:

$$V_{\text{ref}} = V_{\text{BEQ1}} + (2R_c/R_1)(kT/q)\ln n$$  \hspace{1cm} (2)

Adjusting the ratio of $(R_2/R_1)$ could compensate for the first-order linear term of $V_{\text{BE}}$.

2.2 High-order curvature compensation
Considering the full expression of the collector current $I_c$ of BJT and assuming that it’s proportional to some power $m$ of $T$ [2],

$$I_c \propto T^m$$  \hspace{1cm} (3)

an accurate description of the temperature dependence of the base-emitter voltage can be written as:

$$V_{\text{BE}}(T) = V_{g0} \left( 1 - \frac{T}{T_r} \right) + \frac{T}{T_r} V_{\text{BE}}(T_r) - (\eta - m) \frac{kT}{q} \ln \frac{T}{T_r}$$  \hspace{1cm} (4)

where $V_{g0}$ is the extrapolated bandgap voltage at 0 K and $\eta$ is a process-related parameter [22]. $T_r$ is a reference temperature that is typically chosen as room temperature if the temperature ranges from -20 $^\circ\text{C}$ to 80 $^\circ\text{C}$ [23, 24]. The purpose of the compensation is to extract and cancel the last high-order item of Eq. (4). The first-order linear term has been canceled through BGR core. Hence $V_{g0}$ is left, which is the bandgap voltage we want. The compensation procedure is shown in Fig. 3. The final $V_{\text{ref}}$ has been obtained by adding the voltage across $R_2$ generated by $I_{\text{compensation}}$ to the uncompensated one.

The compensation circuit is shown in Fig. 4 with output current $4I_{\text{compensation}}$ on the left, utilizing two important BJTs $Q_8$ and $Q_9$ which have the same size. Giving a constant current to $Q_8$ and a PTAT current to $Q_9$, the $V_{\text{BE}}$ difference between $Q_8$ and $Q_9$ can be written as:

$$V_{\text{BEQ8}} - V_{\text{BEQ9}} = (kT/q)\ln(T/T_r)$$  \hspace{1cm} (5)

That’s the voltage across $R_0$. Assuming the current through $Q_{13}$ and $Q_{14}$ are $I_2$ and $I_1$, the current $I_{\text{compensation}}$ through $R_0$ can be written as:

$$I_{\text{compensation}} = \frac{1}{2}(I_1 - I_2) = \frac{kT}{qR_0} \ln \frac{T}{T_r}$$  \hspace{1cm} (6)

After current copy via BJT, the current through $Q_{18}$ and $Q_{19}$ are $2I_1$ and $2I_2$, respectively. Thus, the output current given to $R_2$ in Fig.2 is $2(I_1-I_2)$. The final output voltage $V_{\text{ref}}$ after compensation can be written as:

$$V_{\text{ref}} = V_{\text{BEQ1}} + (2I_c + 4I_{\text{compensation}})R_2$$

$$= V_{\text{BEQ1}} + 2 \frac{R_2}{R_1} \frac{kT}{q} \ln n + 4 \frac{R_2}{R_0} \frac{kT}{q} \ln \frac{T}{T_r}$$  \hspace{1cm} (7)
The high-order item of $V_{BE}$ could be canceled through Eq. (7).

### 3. Current trimming technique using OTP

Trimming resistors is a typical method of the trimming network. Here proposes a new double-ended current trimming technique as shown in Fig. 5. $I_{trim}$, a portion of PTAT current, is the output current, which is injected into $V_X$ or $V_Y$ in Fig. 2 to adjust the PTAT current across $R_2$. The current trimming block is separated into three parts. The BIT<7:4> current copy part takes $I_{ptat}$ as input and decreases the current by 1/2 in turn. Opamp $A_1$ and $A_2$ are used to make the drain voltage of $M_{12}$ and $M_{17}$ equal to $V_D$ to improve the accuracy of current copy. For the same purpose, bipolar Q20–Q24 as a current mirror is chosen for providing a very high output impedance from the collector of Q21. Further, the BIT<3:0> current copy part decreases the current of $M_{17}$ by increasing the multiplier of $M_{16}$ and then reduces it from $M_{20}$ to $M_{23}$ one by one. $M_{24}$–$M_{27}$ and $M_{28}$–$M_{31}$ act as switches, which are controlled by an 8-bit trim code BIT<0> to BIT<7>. All trim codes are entered through I2C interface circuit, as Fig. 6 shows. The binary code 0 or 1 from the external interface is stored in 8 registers before sending to OTP. If BIT<0> is 0, $x$ varies from 0 to 7, the current in this branch is added to $I_{trim}$, if else, it is injected into GND, which greatly improves the speed of the circuit.

The trimming technique is used to achieve better TC in different corners. If the coefficient of PTAT voltage is larger than that of $V_{BE,Q1}$, $I_{trim}$ will connect to $V_X$ to reduce the PTAT current flows through $R_2$. On the contrary, it will connect to $V_Y$. According to the output voltage as a function of temperature before trimming. ($V_{OUT\_max}$ - $V_{OUT\_min}$) can be written as:

$$V_{OUT\_max} - V_{OUT\_min} = \Delta V = TC \cdot 10^6 \cdot (T_{max} - T_{min}) \cdot V_{avg}$$  \hspace{1cm} (8)

Choosing target TC, the desired $\Delta V_2$ can be written as:

$$\Delta V_2 = TC \cdot 10^6 \cdot (T_{max} - T_{min}) \cdot V_{avg}$$  \hspace{1cm} (9)

The voltage that needs to be trimmed can be estimated as:

$$\Delta V = (\Delta V_1 - \Delta V_2)/2$$ \hspace{1cm} (10)

Combined with the resistance of $R_2$ and maximum current of $I_{trim}$, the trimmed voltage range from -2.6 mV to +2.6 mV.

Except for the current trimming, resistor trimming is also adopted to improve the accuracy of $V_{ref}$. The structure of resistor trimming is shown in Fig. 7, which separates $R_2$ into same resistors. Each resistor connects in parallel with a MOSFET under the control of OTP. The resistance of $R_2$ can be adjusted by controlling whether the MOSFETs are turned on or not.

### 4. Experimental results and discussion

The proposed BGR circuit was fabricated in a 180 nm BCD process and occupied an active area of 0.329 mm², which is shown in Fig. 8. The post-simulation results sh-
ow that the best post-simulated TC of BGR at tt corner is 1.6 ppm/°C, as shown in Fig. 9.

Fig. 10 presents the TC of 10 runs in different corners with a 3.3 V supply voltage. As shown in Fig. 10 (b), TC of 10 runs are all reduced to less than 2 ppm/°C after trimming and all post-trimmed curves have similar shapes.

Fig. 11 shows the 200 Monte Carlo simulation results of $V_{\text{OUT}}$ at 50 °C, 3.3 V. The mean value $\mu$ across 200 runs is about 1.662 V with a standard deviation $\sigma$ of 2.80 mV [30, 31]. Therefore, the $\sigma/\mu$ reaches 0.168%.

To determine trim code, select large samples on a wafer randomly to plot TC distribution. Choose the central value of TC to calculate trim code using Eq. (10). Due to process variation, the calculated results will have a certain deviation. Therefore, test and correct the most appropriate trim code to avoid the repeated burning of OTP on the chip during retest. Afterward, it can be used for all dies in the wafer.

Five chips were chosen to test, the chip microphotograph of BGR is shown in Fig. 12. The measured output voltage at 50 °C with supply voltage varying from 2.9 V to 3.6 V is shown in Fig. 13, which achieves a line sensitivity of 0.18 %/V. Fig. 14 presents the measured output voltage versus temperature [25]. The corresponding measured results after trimming are presented in Fig. 15(b) with all TC less than 10 ppm/°C.

Table 1 summarizes the performance of the proposed BGR in comparison to other reported results. Compared with [28, 29, 30], the proposed BGR achieves a best TC of 2.2 ppm/°C after trimming. And it obtains a wider temperature range than [27, 28, 29, 31]. Besides, it achie-
ves a 0.18 %/V line regulation, which is better than [29].

5. Conclusion

The proposed BGR circuit with a double-ended current trimming technique has been fabricated in a 180 nm BCD process. This technique supports batch trimming, and the obtained trim code could be used for all dies in a wafer. The OTP programming improves the chip and reduces production costs as well. Measurement results show that the BGR achieves a very low temperature coefficient of 2.2 ppm/°C and low line sensitivity of 0.18 %/V.

Acknowledgments

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References


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Table 1 Performance comparison tables.


