2009 International Workshop on Smart Info-Media Systems in Asia (SISA 2009)
Kansai University Centenary Memorial Hall, Osaka, JAPAN

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Sponsored by Smart Info-media Systems Technical Group, The Institute of Electronics, Information and Communication Engineers (IEICE).

Call for Papers

The 2009 International Workshop on Smart Info-Media System in Asia (SISA 2009) is held in Kansai University Centenary Memorial Hall, Osaka, Japan. The SISA 2009 presents every possibility on new information technologies and its smart systems.

The SISA 2009 is aiming at promoting young researchers in the field of multimedia system and wireless communications. We plan to organize poster presentations for regular papers as well as a keynote talk and a special session. Prospective authors are invited to submit their papers reporting original work in these fields.

The topics in SISA 2009 include the followings:

1. Communication Systems
   1.1 Smart Wireless Systems, Smart Mobile Systems
   1.2 Cognitive Systems, Intelligent Soft-Wireless Systems
   1.3 Multi-Media over Wireless
   1.4 Signal Processing for Communication Systems
   1.5 Intelligent Communication Systems,
   1.6 Ultra Wideband Communications
   1.7 RFID, Sensor Networks
   1.8 WAM/MAN/LAN/PAN
   1.9 Others

2. Multimedia and Systems
   2.1 Speech Processing and Coding
   2.2 Video Processing and Coding
   2.3 Video and Multimedia Technology & Communications
   2.4 Audio/Acoustic Signal Processing
   2.5 Multimedia Processing for e-Learning
   2.6 Intelligent Signal Processing for Multimedia & Systems
   2.7 Security Signal Processing for Multimedia & Systems
   2.8 Others

Authors are invited to submit a full paper in accordance with posted guidelines. Only electronic submissions will be accepted via our website at: http://splab.cs.kitami-it.ac.jp/sisa2009/

Author’s Schedule:
Deadline for Submission of Regular Paper: June 8, 2009
Notification of Acceptance: August 7, 2009
Deadline for Submission of Camera Ready Paper: September 7, 2009

We plan to publish a Special Section on IEICE Trans. Fundamentals on October 2010. Authors who presented their original works in SISA 2009 are solicited to submit papers to this special section.
Call for Papers
ASP-DAC 2010
Asia and South Pacific Design Automation Conference 2010
http://www.aspdac.com/aspdac2010/
January 18-21, 2010
Taipei, Taiwan

Aims of the Conference:
ASP-DAC 2010 is the fifteenth annual international conference on VLSI design automation in Asia and South Pacific region, one of the most active regions of design and fabrication of silicon chips in the world. The conference aims at providing the Asian and South Pacific CAD/DA and Design community with opportunities of presenting recent advances and with forums for future directions in technologies related to Electronic Design Automation (EDA). The format of the meeting intends to cultivate and promote an instructive and productive interchange of ideas among EDA researchers/developers and system/circuit/device designers. All scientists, engineers, and students who are interested in theoretical and practical aspects of VLSI design and design automation are welcomed to ASP-DAC.

Areas of Interest:
Original papers on, but not limited to, the following areas are invited. Please note that ASP-DAC will work cooperatively with other conferences and symposia in the field to check for double submissions.

[1] System-Level Modeling and Simulation/Verification:
- System-level modeling, specification, language, performance analysis, system-level simulation/verification, hardware-software co-simulation/co-verification, etc.

[2] System-Level Synthesis and Optimization:
- System-on-chip and multi-processor SoC (MPSoc) design methodology, hardware-software partitioning, hardware-software co-design, IP/platform-based design, application-specific instruction-set processor (ASIP) synthesis, low power system design, etc.

[3] System-Level Memory/Communication Design and Networks on Chip:
- Communication-based architecture design, network-on-chip (NoC) design methodologies and CAD, interface synthesis, system communication architecture, memory architecture, low power communication design, etc.

- Embedded system design, real-time system design, OS, middleware, compilation techniques, memory/cache optimization, interfacing and software issues.

[5] High-Level/Behavioral/Logic Synthesis and Optimization:
- High-Level/behavioral/RTL synthesis, technology-independent optimization, technology mapping, interaction between logic design and layout, sequential and asynchronous logic synthesis, resource scheduling, allocation, and synthesis.

[6] Validation and Verification for Behavioral/Logic Design:
- Logic simulation, symbolic simulation, formal verification, equivalence checking, transaction-level/RTL and gate-level modeling and validation, assertion-based verification, coverage-analysis, constrained-random testbench generation.

[7] Physical Design:
- Floorplanning, partitioning, placement, buffer insertion, routing, interconnect planning, clock network synthesis, post-placement optimization, layout verification, package/PCB routing, etc.

[8] Timing, Power, Thermal Analysis and Optimization:
- Deterministic and statistical static timing analysis, statistical performance analysis and optimization, low power design, power and leakage analysis, power/ground and package analysis and optimization, thermal analysis, etc.

[9] Signal/Power Integrity, Interconnect/Device/Circuit Modeling and Simulation:
- Signal/power integrity, clock and bus analysis, interconnect and substrate modeling/extraction, package modeling, device modeling/simulation, circuit simulation, high-frequency and electromagnetic simulation of circuits, etc.

[10] Design for Manufacturability/Yield and Statistical Design:
- DFM, DFY, CAD support for OPC and RET, variability analysis, yield analysis and optimization, reliability analysis, design for resilience and robustness, cell library design, design fabrics, etc.

[11] Test and Design for Testability:
- Testable design, fault modeling, ATPG, BIST and DFT, memory test and repair, core and system test, delay test, analog and mixed signal test.

[12] Analog, RF and Mixed Signal Design and CAD:
- Analog/RF synthesis, analog layout, verification and simulation techniques, noise analysis, mixed-signal design considerations.

[13] Emerging technologies and applications:
i. Design case studies for emerging applications: multimedia, consumer electronics, communication, networking, ubiquitous computing and biomedical applications, etc.
ii. Post CMOS technologies: nanotechnology, quantum optical interconnect, 3D integration, probabilistic architecture, microfluidics, molecular, bioelectronics, etc., with emphasis on modeling, analysis, novel circuit/architecture, CAD tools, and design methodologies.

Submission of Papers:
Deadline for submission: 5 PM JST (GMT+9) Aug. 3 (Mon.), 2009
Notification of acceptance: 5 PM JST (GMT+9) Sept. 25 (Fri.), 2009
Deadline for final version: 5 PM JST (GMT+9) Nov. 16 (Mon.), 2009

Specification of the paper submission format will be available at the WEB site:
http://www.aspdac.com/aspdac2010/

Panels, Special Sessions and Tutorials:
Suggestions and proposals are welcome and have to be addressed to the Conference Secretariat (e-mail: aspdac2010@aspdac.com) no later than June 8 (Mon.), 2009.

Prospective Sponsors:
ACM SIGDA, IEEE Circuits and Systems Society

ASP-DAC2010 Chairs:
General Chair: Youn-Long Lin (National Tsing Hua Univ.)
Technical Program Chair: Shoji Kimura (Waseda Univ.)
Technical Program Vice Chairs: Hyunchul Shin (Hanyang Univ.) and Jing-Jia Liou (National Tsing Hua Univ.)

Contact:
Conference Secretariat: aspdac2010@aspdac.com
TPC Secretariat: aspdac2010tpc@mls.aspdac.com
CALL FOR PAPERS

ISCAS 2010

May 30th - June 2nd 2010
Paris, France

Nanoelectronics and Nano-Technology on Circuits and Systems

2010 IEEE International Symposium on Circuits and Systems

The IEEE International Symposium on Circuits and Systems (ISCAS) is the world's premier networking forum of leading researchers in the highly active fields of theory, design and implementation of circuits and systems. ISCAS 2010, sponsored by the IEEE Circuits and Systems Society and supported by the Institut Supérieur d'Électronique de Paris, will be held in Paris, France from 30 May to 2 June 2010. The Symposium will focus on circuits and systems employing nanodevices (both extremely scaled CMOS and non-CMOS devices) and circuit fabrics (mixture of standard CMOS and evolving nano-structure elements) and their implementation cost, switching speed, energy efficiency, and reliability. The ISCAS 2010 will include oral and poster sessions; tutorials given by experts in state-of-the-art topics; and special sessions, with the aim of complementing the regular program with topics of particular interest to the circuits and systems community that cut across and beyond disciplines traditionally represented at ISCAS. Prospective authors are invited to submit papers as well as tutorial reviews on circuits and systems topics including but not limited to:

- Analog Signal Processing
- Biomedical Circuits and Systems
- Cellular Neural Networks and Array Computing
- Circuits and Systems for Communications
- Computer-Aided Network Design
- Digital Signal Processing
- Education in Circuits and Systems
- Life Demonstrations of Circuits and Systems
- Life-Science Systems and Applications
- Multimedia Systems and Applications
- Nanoelectronics and Gigascale Systems
- Neural Systems and Applications
- Nonlinear Circuits and Systems
- Power Systems and Power Electronic Circuits
- Sensory Systems
- Visual Signal Processing and Communications
- VLSI Systems, Architectures and Applications
- Circuits and Systems for Wearable Computing

Authors are invited to submit a 4-page Full Paper according to posted guidelines. Only electronic submissions will be accepted via the Web at http://www.iscas2010.org/. At least one author of each paper must register for the Symposium by 12 February 2010 for papers to be included in the program. Authors are expected to present their papers at the Symposium. Best Student Paper Contest: ISCAS 2010 will sponsor a student paper contest. To qualify, a student or group of students must be the primary author(s). The submissions for the student paper contest should be clearly indicated. The papers will be judged based on both content and presentation. Social Activities: Besides the technical program, a very entertaining social program is planned. Special tours to tourist attractions will be available to the Symposium attendees and their guests.

Deadline for submission of Tutorial Proposals: 11 September 2009
Deadline of submission of Special Sessions Proposals: 11 September 2009
Notification of acceptance of Special Sessions Proposals: 2 October 2009
Deadline for submission of Full 4-page Papers in Regular Sessions: 9 October 2009
Deadline for submission of Full 4-page Papers in Special Sessions: 30 October 2009
Notification of Paper Acceptance: 8 January 2010
Deadline for Submission of FINAL Papers: 12 February 2010
Deadline for Author Registration: 12 February 2010
第32回情報理論とその応用シンポジウム（SITA2009）

開催期間  平成21年12月1日（火）～平成21年12月4日（金）
開催場所  ホテルかめ福 〒753-0056 山口県山口市湯田温泉 4-5

日程
8月5日（水） 参加・発表・宿泊申し込み 受付開始
9月18日（金） 発表申し込み 締め切り
10月5日（月） 原稿 締め切り

主催  情報理論とその応用学会
共催  IEEE Information Theory Society, Japan Chapter
協賛  電子情報通信学会 基礎・境界ソサイエティ
後援  山口大学工学部
山口県光コンベンション協会
運営組織  実行委員長 柳研二郎（山口大学）
            プログラム委員長 岡育生（大阪市立大学）
SITA2009事務局 〒755-8611 山口県宇部市常盤台2-16-1

SITA2009実行委員長
柳 研二郎

詳細は以下のホームページを参照お願います:

SITA2009
2010 IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP)
Sheraton Dallas Hotel
March 15 – 19, 2010 • Dallas, Texas, USA
www.ICASSP2010.com

Welcome to Texas, Y’All! Dallas is known for living large and thinking big. As the nation’s ninth-largest city, Dallas is exciting, diverse and friendly - factors that contribute to its success as a leading leisure and convention destination. There’s a whole “new” vibrant Dallas to enjoy-new entertainment districts, dining, shopping, hotels, arts and cultural institutions- with more on the way. There’s never been a more exciting time to visit Dallas than now.

Submission of Papers: Prospective authors are invited to submit full-length, four-page papers, including figures and references, to the ICASSP Technical Committee. All ICASSP papers will be handled and reviewed electronically. The ICASSP 2010 website www.icassp2010.com will provide you with further details. Please note that all submission deadlines are strict.

Tutorial and Special Session Proposals: Tutorials will be held on March 14 and 15, 2010. Brief proposals should be submitted by July 31, 2009, to tutorials@icassp2010.com and must include title, outline, contact information for the presenter, and a description of the tutorial and material to be distributed to participants. Special sessions proposals should be submitted by July 31, 2009, to specialsessions@icassp2010.com and must include a topical title, rationale, session outline, contact information, and a list of invited papers. Tutorial and special session authors are referred to the ICASSP website for additional information regarding submissions.

Important Deadlines

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