Call for Papers
ASP-DAC 2011
Asia and South Pacific Design Automation Conference 2011
http://www.aspdac.com/aspdac2011/
January 25-28, 2011
Yokohama, Japan

Aims of the Conference:
ASP-DAC 2011 is the sixteenth annual international conference on VLSI design automation in Asia and South Pacific region, one of the most active regions of design and fabrication of silicon chips in the world. The conference aims at providing the Asian and South Pacific CAD/DA and Design community with opportunities of presenting recent advances and with forums for future directions in technologies related to Electronic Design Automation (EDA). The format of the meeting intends to cultivate and promote an instructive and productive interchange of ideas among EDA researchers/developers and system/circuit/device designers. All scientists, engineers, and students who are interested in the theoretical and practical aspects of VLSI design and design automation are welcomed to ASP-DAC.

Areas of Interest:
Original papers on, but not limited to, the following areas are invited.

1. System-Level Modeling and Simulation/Verification:
   - System-level modeling, specification, language, performance analysis, system-level simulation/verification, hardware-software co-simulation/co-verification, etc.

2. System-Level Synthesis and Optimization:
   - System-on-chip and multi-processor SoC (MPSoC) design methodology, hardware-software partitioning, hardware-software co-design, IP/platform-based design, application-specific instruction-set processor (ASIP) synthesis, low-power system design, etc.

3. System-Level Memory/Communication Design and Networks on Chip:
   - Communication-based architecture design, network-on-chip (NoC) design methodologies and CAD, interface synthesis, system communication architecture, memory architecture, low-power communication design, etc.

4. Embedded and Real-Time Systems:
   - Embedded system design, real-time system design, OS, middleware, compilation techniques, memory/cache optimization, interfacing and software issues.

5. High-Level/Behavioral/Logic Synthesis and Optimization:
   - High-level/behavioral/RTL synthesis, technology-independent optimization, technology mapping, interaction between logic design and layout, sequential and asynchronous logic synthesis, resource scheduling, allocation, and synthesis.

6. Validation and Verification for Behavioral/Logic Design:
   - Logic simulation, symbolic simulation, formal verification, equivalence checking, transaction-level/RTL and gate-level modeling and validation, assertion-based verification, coverage analysis, constrained-random testbench generation.

7. Physical Design:
   - Floorplanning, partitioning, placement, buffer insertion, routing, interconnect planning, clock network synthesis, post-placement optimization, layout verification, etc.

8. Timing, Power, Thermal Analysis and Optimization:
   - Deterministic and statistical static timing analysis, statistical performance analysis and optimization, low power design, power and leakage analysis, power/ground and package analysis and optimization, thermal analysis, etc.

9. Signal/Power Integrity, Interconnect/Device/Circuit Modeling and Simulation:
   - Signal/power integrity, clock and bus analysis, interconnect and substrate modeling/extraction, package modeling, device modeling/simulation, circuit simulation, high-frequency and electromagnetic simulation of circuits, etc.

10. Design for Manufacturability/Yield and Statistical Design:
    - DFM, DFY, CAD support for OPC and RET, variability analysis, yield analysis and optimization, reliability analysis, design for resilience and robustness, cell library design, design fabrics, etc.

11. Test and Design for Testability:
    - Testable design, fault modeling, ATPG, BIST and DFT, memory test and repair, core and system test, delay test, analog and mixed signal test.

12. Analog, RF and Mixed Signal Design and CAD:
    - Analog/RF synthesis, analog layout, verification and simulation techniques, noise analysis, mixed-signal design.

13. Emerging technologies and applications
    i. Design case studies for emerging applications: multimedia, consumer electronics, communication, networking, ubiquitous computing and biomedical applications, etc.
    ii. Post CMOS technologies: nanotechnology, quantum, optical interconnect, 3D integration, probabilistic architecture, microfluidics, molecular, bioelectronics, etc., with emphasis on modeling, analysis, novel circuit/architecture, CAD tools, and design methodologies.

Paper Submission Deadline:
July 19, 2010, 5:00 PM JST (GMT +09:00)

Panels, Special Sessions and Tutorials:
Suggestions and proposals are welcome and have to be addressed to the Conference Secretariat (e-mail: aspdac2011-sec@mls.aspdac.com) no later than June 7 (Mon.), 2010.

Prospective Sponsors:
ACM SIGDA, IEEE Circuits and Systems Society

ASP-DAC2011 Chairs:
General Chair: Kunihiro Asada(Univ. of Tokyo)
Technical Program Chair: Hyunchul Shin (Hanyang Univ.)

Contact:
Conference Secretariat: aspdac2011-sec@mls.aspdac.com
TPC Secretariat: aspdac2011-tpc@mls.aspdac.com
Call for Designs
University LSI Design Contest
ASP-DAC 2011
http://www.aspdac.com/aspdac2011/
January 25-28, 2011
Yokohama, Japan

Aims of the Contest:
As a unique feature of ASP-DAC 2011, the University LSI Design Contest will be held. The aim of the Contest is to encourage education and research on VLSI design at universities and other educational organizations. We solicit designs that fit in one or more of the following categories:

1. Designed, and actually implemented on chips in universities or other educational organizations during the last two years;
2. Designs that report actual measurements from implementations;
3. Innovative design prototypes.

Interesting or excellent designs selected will be honored by providing the opportunities for presentation in a special session at the conference. Award(s) will be given to a few numbers of outstanding designs, selected from those presented at the conference.

Areas of Design:
Application areas or types of circuits of the original LSI circuit designs include (but are not limited to):
Methods or technology used for implementation include:
(a) Full Custom and Cell-Based LSIs, (b) Gate Arrays, (c) FPGA/PLDs.

Submission of Design Descriptions:
A camera-ready summary is requested to be prepared within 2 pages including figures, tables, and references. It is strongly recommended that measured experimental results and a chip micrograph are included in the original LSI circuit design. Please do not submit the same paper as a regular paper.

Specification of the submission format will be available at http://www.aspdac.com/aspdac2011/

Deadline for summary: 5PM JST (GMT+9) July 19 (Mon.), 2010
Notification of acceptance: Sep. 24 (Fri.), 2010
Deadline for camera-ready: 5PM JST (GMT+9) Nov. 15 (Mon.), 2010

Review:
Submitted designs will be reviewed by the Design Contest Committee in a process similar to the review process for the technical papers. The following criteria will be applied in the selection of designs:
Interesting or excellent designs selected will be presented at a special session of the conference.

Presentation:
An author of each selected design will be required to make a short presentation at a special session of ASP-DAC 2011. A digest of each design to be presented will be included in the conference proceedings.

Contact Email: aspdac2011-udc@mls.aspdac.com

ASP-DAC 2011 Chairs
General Chair: Kunihiro Asada (University of Tokyo)
Technical Program Chair: Hyunchul Shin (Hanyang University)
Design Contest Co-Chairs: Masanori Hariyama (Tohoku University), Hiroshi Kawaguchi (Kobe University)
第 33 回情報理論とその応用シンポジウム開催案内

ご挨拶

第 33 回情報理論とその応用シンポジウム（SITA2010）を長野市松代で開催致します。会場の位置する松代町は、江戸時代に信濃国随一の藩、松代藩の城下町があった場所で、現在でも歴史を感じさせる町並みが一部に残っています。また、松代温泉と呼ばれる温泉があり、タオルが染まるほどの茶色のお湯が特徴です。多数の方々のご参加をお待ちしております。

SITA2010 実行委員長 杉村立夫

主な日程

8 月 2 日（月） 参加・発表・宿泊申し込み受付開始
9 月 1 日（水） 発表申し込み締め切り
9 月 30 日（木） 論文原稿締め切り

ホームページ

http://www.sita.gr.jp/SITA2010/

共催

情報理論とその応用学会

協賛

IEEE Information Theory Society, Japan Chapter

運営組織

実行委員長 杉村立夫（信州大学）
プログラム委員長 森田啓義（電気通信大学）

SITA2010 事務局

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第 33 回情報理論とその応用シンポジウム

開催期間

2010 年 11月 30 日（火）～12月 3 日（金）

開催場所

信州松代ロイヤルホテル
長野県長野市松代町西寺尾 1372-1

分野

シャノン理論、情報源符号化、データ圧縮、確率過程、符号理論、通信路符号化、符号化変調、系列、スペクトル拡散通信、通信方式、光通信理論、検定と推定、暗号、情報セキュリティ、情報ネットワーク、ネットワーク符号化、情報理論応用、量子情報理論、画像・音声処理、信号処理、パターン認識と学習、量子符号・暗号、記録素子用の符号化・信号処理、エントロピーと情報量、情報理論基礎、その他
2011 IEEE International Symposium on Circuits and Systems

The IEEE International Symposium on Circuits and Systems (ISCAS) is the world’s premier networking forum of leading researchers in the highly active fields of theory, design and implementation of circuits and systems.

ISCAS 2011, sponsored by the IEEE Circuits and Systems Society and supported by the Federal University of Rio de Janeiro (UFRJ), Brazil and the Military Institute of Engineering (IME), will be held in Rio de Janeiro, Brazil, from 15 May to 18 May 2011.

The Symposium will focus on Circuits and Systems for Sustainable Environment, employing nanotechnology, sensor arrays, mobile processing, and energy-efficient systems, aiming at the natural equilibrium of planet earth. The ISCAS 2011 will include, oral and poster sessions, tutorials given by experts on state-of-the-art topics, and special sessions, with the aim of complementing the regular program with topics of particular interest to the circuits and systems community that cut across and beyond disciplines traditionally represented at ISCAS.

Prospective authors are invited to submit papers including technical novelties and tutorial overviews on circuits and systems topics (including but not limited to):

- Analog Signal Processing
- Biomedical Circuits and Systems
- Cellular Neural Networks and Array Computing
- Circuits and Systems for Communications
- Circuits and Systems for Video Technology
- Computer-Aided Network Design
- Digital Signal Processing
- Education in Circuits and Systems
- Education in Circuits and Systems
- Life-Science Systems and Applications
- Multimedia Systems and Applications
- Nanoelectronics and Gigascale Systems
- Neural Systems and Applications
- Nonlinear Circuits and Systems
- Power Systems and Power Electronic Circuits
- Sensory Systems
- Visual Signal Processing and Communications
- VLSI Systems and Applications

Potential authors for regular papers, live demos (see separate call for live demos), tutorials, and special sessions are invited to visit the conference website http://www.iscas2011.org and click on the corresponding links for details.

For regular sessions, authors are invited to submit 4-page full papers according to the posted guidelines. If the papers belong to live demonstrations, the authors should provide one additional demo requirement page along with the 4-page paper for regular technical tracks during the submission.

Only electronic submissions will be accepted via the Web at: http://www.epapers.org/iscas2011.

Authors of accepted papers are expected to present their papers at the Symposium and at least one author of each paper MUST register by 21 January 2011 in order for the papers to be included in the program.

Best Student Paper Contest: ISCAS 2011 will sponsor a student paper contest. To qualify, a student or group of students must be the primary author(s). Submissions for the student’s paper contest shall be clearly indicated. The papers will be judged based on both content and presentation.

Social Activities: Besides the technical program, a very entertaining social program is planned. Special tours to Rio’s attractions will be available to the Symposium attendees and their guests.

Important dates

<table>
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<tr>
<th>Event</th>
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<tr>
<td>Deadline for submission of Tutorial Proposals</td>
<td>10 September 2010</td>
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<tr>
<td>Notification for acceptance for Special Session Proposals</td>
<td>22 September 2010</td>
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<tr>
<td>Deadline for submission of Full 4-page Papers in Regular Sessions</td>
<td>29 September 2010</td>
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<tr>
<td>Deadline for submission of Full 4-page Papers in Special Sessions</td>
<td>29 October 2010</td>
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<tr>
<td>Notification of Paper Acceptance</td>
<td>17 December 2010</td>
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The 36th International Conference on Acoustics, Speech, and Signal Processing (ICASSP) will be held at the Prague Congress Center, May 22–27, 2011.

The ICASSP meeting is the world's largest and most comprehensive technical conference focused on signal processing and its applications. The conference will feature world-class speakers, tutorials, exhibits, and over 120 lecture and poster sessions on the following topics:

- Audio and Acoustic Signal Processing
- Bio Imaging and Signal Processing
- Design and Implementation of Signal Processing Systems
- Image, Video, and Multidimensional Signal Processing
- Industry Technology Tracks
- Information Forensics and Security
- Machine Learning for Signal Processing
- Multimedia Signal Processing
- Sensor Array and Multichannel Systems
- Signal Processing Education
- Signal Processing for Communications and Networking
- Signal Processing Theory and Methods
- Speech Processing
- Spoken Language Processing

WELCOME TO PRAGUE
Prague, the capital of the Czech Republic, is a beautiful city rich in history and architecture. It has become a cultural, political, and scientific heart of the Czech Republic. Visitors soon appreciate the term “golden city” or the “city of a hundred spires”.

SUBMISSION OF PAPERS
Prospective authors are invited to submit full-length, four-page papers, including figures and references through the web site www.icassp2011.com. The web site will provide further details. Please note that all submission deadlines are strict.

Special Session & Tutorial Proposals Due September 1, 2010
Notification of Special Session & Tutorial Acceptance October 6, 2010
Submission of Camera Ready Papers October 20, 2010
Notification of Paper Acceptance January 17, 2011
Revised Paper Upload Deadline February 20, 2011
Registration Deadline for Authors March 13, 2011