A 1-Dimensional Chaotic IC Designed by SI Techniques

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In this paper, a VLSI chip of a discrete-time chaos circuit realizing a tent map is reported. The VLSI chip is fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC). A simple structure enables us to realize the circuit with 10 MOSFET's and 2 capacitors. Furthermore, the circuit which is designed by switched-current (SI) techniques can operate at 3V power supply. The experiment concerning the VLSI chip shows that the proposed circuit is integrable by a standard 1.2 μ m CMOS technology.

Keywords: integrated circuit, chaotic IC's, switched current, discrete-time circuits, analog circuits

1. Introduction

In the field of engineering, biology, physics, and so on, chaos and its applications are becoming important since chaotic phenomenon is frequently encountered in many nonlinear dynamical systems. For investigating these nonlinear dynamical systems, it is advisable to use simple chaos circuits since the investigation employing digital computers requires long computational time. Being distinct from above-mentioned purpose, the chaos circuit which has a simple structure is useful as a building block of chaos application systems. For example, chaotic signals are used as annealing noise for neural networks, spread signals for chaos-based communication systems, etc. ^{(1)~(3)}. For above-mentioned reasons, many types of chaos circuits have already been reported for the monolithic IC realization ^{(4)~(6)}. However, most of these circuits require high power supply, e.g. the supply voltage $V_{dd} = 10V$. In the realization of the integrated analog circuits, need of low-voltage design has been increasing. Down-scaling into sub-microns in advanced VLSI fabrication technologies demands lowering of supply voltages. To exploit as a building block for complex applications systems, not only the chaos circuits should have a simple structure, but they must be compatible with a low-voltage realization.

In this paper, a VLSI chip of a discrete-time chaos circuit realizing a tent map is reported. The VLSI chip is fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC). The circuit which has a simple structure can be constructed with 10 MOSFET's and 2 capacitors. Furthermore, the circuit designed using switched-current (SI) techniques can oper-

ate at 3V power supply. To confirm the validity of the circuit design, computer simulations and experiments are performed.

2. Circuit Structure

Figure 1 shows the proposed chaos circuit realizing a tent map. The design of the proposed SI chaos circuit is based on

$$X(t+1) = F(X(t)), \\ = 2\{X(t) - 2(X(t) \ominus 0.5)\}, \dots\dots\dots (1)$$

where $\ominus$ is a bounded difference operator. In Fig.1, the initial value $X(0)$ is given by V_{in} in the track & hold block. When Φ is *off* and $\bar{\Phi}$ is *on*, the signal $X(t)$ which corresponds to the charged voltage in C_1 is provided for the bounded-difference circuit via M1 and M2. Then the bounded-difference block operates $X(t) - 2(X(t) \ominus I_1)$. In this block, the constant 0.5 in Eq.(1) corresponds to the current source I_1 , and the multiplication is realized by the current-copying ratio of M3 and M4. The output

Fig.1. Proposed chaos circuit realizing a tent map.

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Fig. 2. Photograph of the fabricated IC.

of the bounded-difference block is charged in C_2 . After the states of the clock pulses are reversed, the signal $X(t) - 2(X(t) \ominus I_1)$ which is charged in C_2 is multiplied by the current-mirror which is composed of M5 and M6. The multiplied signal $2\{X(t) - 2(X(t) \ominus I_1)\}$ is charged in C_1 as $X(t+1)$.

As Fig.1 shows, the circuit consists of 10 MOSFET's and 2 capacitors. The number of MOSFET's used in the proposed circuit is about 50%[†] of that used in the previous circuit proposed in⁽⁷⁾.

3. IC Implementation

3.1 Layout Design The proposed circuit was implemented by a 1.2 μm CMOS process. Figure 2 shows the photograph of the fabricated IC. The VLSI chip shown in Fig.2 was fabricated in the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo with the collaboration by On-Semiconductor, Nippon Motorola LTD., HOYA Corporation, and KYOCERA Corporation. The size for a circuit is less than $150\mu\text{m} \times 90\mu\text{m}$.

3.2 Experiment The experiments were performed concerning the fabricated VLSI chip. Figures 3 and 4 show the measured nonlinear function and chaotic signal, respectively. The experiments were performed under the conditions that $V_{dd} = 3\text{V}$, $I_1 = 10\mu\text{A}$, and $C1 = C2 = 10\text{nF}$ ^{††}. In the experiment, the clock frequency was set to 100 Hz.

4. Conclusion

A VLSI chip of a discrete-time chaos circuit has been reported in this paper. The circuit realizing a tent map was designed using a switched-current technique.

The experiments concerning the fabricated chip showed that 1. the fabricated IC can operate at 3V power supply and 2. the small size can be achieved since the circuit is integrable with 10 MOSFET's and 2 capacitors.

The proposed SI chaos circuit can be implemented by

[†]The conventional circuit is composed of 25 MOSFET's and 2 capacitors.

^{††}Although the fabricated IC includes capacitors, the external capacitors were used in the experiments. Because of the effect of noise, the chaotic signals could not be measured without the external capacitors.

Fig. 3. Measured nonlinear function.

Fig. 4. Measured chaotic signal.

a standard CMOS technology.

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