Design of a Step-Down Switched-Capacitor DC-DC Converter with Charge-Average Processes

Kei Eguchi∗ Member
Shinya Terada** Non-member
Fumio Ueno** Member
Hongbing Zhu*** Member
Toru Tabata∗ Non-member
Takahiro Inoue**** Member

A step-down DC-DC converter with charge-average processes is proposed in this paper. The converter is designed by using switched-capacitor (SC) techniques. Different from conventional converters such as a series-parallel type power converter and a Dickson-type power converter, the ripple noise of the proposed converter is small, because the output voltage is always obtained irrespective of the states of the clock pulses. The output voltage of the proposed converter is expressed by \((Q/P) \times V_{\text{in}}\) \((P \in \{1, 2, \ldots, N\}\) and \(Q \in \{1, 2, \ldots, N\}\). Furthermore, when the number of the capacitors is small, the hardware-cost for the proposed circuit is less than that for the conventional converters such as a series-parallel type power converter and a ring-type power converter. Concerning 3-stage power converters, SPICE simulations are performed to confirm the validity of the circuit design. For the input voltage 3.6 V, the power efficiency of the proposed circuit is 92.7 % in the output current about 320 mA.

Keywords: DC-DC converters, switched-capacitor circuits, bootstrap circuits, cellular phones, discrete-time circuits

1. Introduction

In the design of power converters for mobile equipments such as cellular phones and digital cameras, needs for thin circuit composition and light-weight are growing. Most of the power transformers exploit magnetic elements to converter input voltages. However, the magnetic elements such as inductors cause the increase of volume and weight, and there is the possibility of faulty operation for neighboring circuits. Therefore we focused on a switched-capacitor (SC) technique. The power converters which are designed by using SC techniques consist of only power-switches and capacitors\(^{(1)-(17)}\). For the realization of the SC power transformers, several attempts have already been made. For example, Mak et al. realized a series-parallel type power converter\(^{(3)}\), and Hara et al. proposed a ring-type type DC-DC converter\(^{(13)}\). However, different from the power transformers using magnetic elements, the SC power transformers cannot convert the voltage continuously. In the design of a cellular phone, the DC voltage such as 2.3 V is required for CPU’s. Therefore the SC DC-DC converters which can generate 2/3 stepped-down voltages are required to realize high efficiency, because the typical voltage of the lithium battery is about 3.6 V.

In this paper, a step-down DC-DC converter with charge-average processes is proposed. The converter designed by using switched-capacitor (SC) techniques can generate the output voltage which is expressed by \((Q/P) \times V_{\text{in}}\) \((P \in \{1, 2, \ldots, N\}\) and \(Q \in \{1, 2, \ldots, N\}\)). Different from conventional converters such as a series-parallel type power converter\(^{(15)-(14)}\) and a Dickson-type power converter\(^{(5)-(12)}\), the ripple noise of the proposed converter is small, because the output voltage is always obtained irrespective of the states of the clock pulses. Furthermore, when the number of the capacitors is small, the hardware-cost for the proposed circuit is less than that for the conventional converters such as a series-parallel type power converter and a ring-type power converter\(^{(13)-(16)}\). Concerning 3-stage power converters, SPICE simulations are performed to confirm the validity of the circuit design.

2. Circuit Structure

2.1 Series-Parallel type DC-DC Converter

Figure 1 shows a series-parallel type power converter\(^{(3)-(4)}\). The conventional converter shown in Fig.1 can provide stepped-up and stepped-down voltages. The conventional converter consists of \(4N - 1\) power switches and \(N + 1\) capacitors. However series-parallel type con-
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Fig. 1. Series-parallel type power converter

Fig. 2. Series-parallel type power converter for step-down conversion

In Fig. 2, the power-switches \( S_{i,j} \) are driven by non-overlapped 2-phase pulses \( \Phi_{i,j} \). Firstly, the capacitors \( C_1, \ldots, C_P \) are connected in series via \( S_{2,j} \). In this timing, the charged-voltage of each capacitor becomes \( V_{in}/P \) since \( C_1, \ldots, C_P \) are charged by the input voltage \( V_{in} \) via \( S_{3,j} \) and \( S_{4,j} \). Next, \( C_1, \ldots, C_P \) are connected in parallel via \( S_{1,j} \) and \( S_{4,j} \). In this timing, the output voltage \( V_{in}/P \) is obtained. The step-down conversion is achieved by iterating these operations. Hence, in the series-parallel type converter, the output capacitor \( C_o \) becomes large to reduce the ripple noise of the output voltage, because the output voltage cannot be obtained in every clock cycle.

When the output current is 0 and the voltage-drop caused by power-switches is free, the output voltage \( V_{out} \) is given by

\[
V_{out} = \frac{1}{P} V_{in}, \quad \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots (1)
\]

where \( P \in \{1,2,\ldots,N\} \). As Eq.(1) shows, the series-parallel type power converter cannot provide a 2/3 stepped-down voltage.

2.2 Ring type DC-DC Converter

Figure 3 shows a ring-type power converter (13)-(16). The conventional converter consists of \( 4N \) power switches and \( N+1 \) capacitors. In Fig. 3, the clock pulses for \( S_{1,j} \) are non-overlapped \( N \)-phase pulses \( \Phi_{i,j} \) ( \( i = 1, \ldots, 4 \) and \( j = 1,2,\ldots,N \) ), and the clock pulses for \( S_{2,j} \) are set to the inverted pulses of \( \Phi_{i,j} \). The switches \( S_{3,j} \) and \( S_{4,j} \) are driven by the clock pulses obtained by shifting the clock-pulses \( \Phi_{i,j} \) cyclically. When \( P \) capacitors are connected in series via \( S_{3,j} \), \( S_{2,j} \), and \( S_{1,j} \), the charged-voltage of each capacitor becomes \( V_{in}/P \). At the same time, \( Q \) capacitors in the series-connected capacitors are connected to the output terminal via \( S_{4,j} \). Hence, the output voltage \( V_{out} \) is given by

\[
V_{out} = \frac{Q}{P} V_{in}, \quad \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots (2)
\]

where \( P \) and \( Q \in \{1,2,\ldots,N\} \) denote the number of the capacitors connected to the input terminal and the output terminal, respectively. The parameters \( P \) and \( Q \) are determined by the timing of the clock pulses for \( S_{3,j} \) and \( S_{4,j} \), respectively. As Eq.(2) shows, the ring-type power converter can generate various types of output voltages.

Different from the series-parallel type converter, the output voltage of the ring-type converter is always obtained irrespective of the states of the clock pulses. Therefore the ripple noise of the ring-type converter is smaller than that of the series-parallel type converter. However, as Figs.1 ~ 3 show, the hardware-cost for the ring-type power converter is larger than that for the series-parallel type. Furthermore, the control of the power-switches is complex since the ring-type power converter requires \( N \)-phase clock pulses.
The proposed converter consists of \(2^N\) power switches and \(N\) capacitors, respectively. When \(N = 3\), the electric charges in the input and the output voltages of the proposed converter is always obtained irrespective of the states of the clock pulses.

When the voltage drops caused by the power switches are 0, the characteristics of Figs.7 (a) and (b) can be analyzed as follows. In the steady state, the differential values of the electric charges in \(C_k\) \((k=1,\ldots,P)\) and \(C_o\) satisfy

\[
\Delta \Phi_{k,\text{in}} + \Delta \Phi_{k,\text{out}} = 0, \quad \ldots \ldots \hspace{1cm} (3)
\]

where \(\Delta \Phi_{k,\text{in}}\) and \(\Delta \Phi_{k,\text{out}}\) denote the electric charges when \(\Phi_1\) and \(\Phi_2\), respectively. In the case of \(\Phi_1\), the differential values of the electric charges in the input and the output terminals, \(\Delta \Phi_{1,\text{in}}\) and \(\Delta \Phi_{1,\text{out}}\), are given by

\[
\Delta \Phi_{1,\text{in}} = \Delta \Phi_{1}^k, \quad \text{and} \quad \Delta \Phi_{1,\text{out}} = \Delta \Phi_{1}^{p_k} + \Delta \Phi_{1}^{q_k} - \Delta \Phi_{1}^1 = \Delta \Phi_{1}^p + \Delta \Phi_{1}^{q_k} - \Delta \Phi_{1}^{p_k-1}, \ldots \hspace{1cm} (4)
\]

On the other hand, in the case of \(\Phi_2\), the differential values of the electric charges in the input and the output terminals, \(\Delta \Phi_{2,\text{in}}\) and \(\Delta \Phi_{2,\text{out}}\), are given by

\[
\Delta \Phi_{2,\text{in}} = \Delta \Phi_{2,\text{in}} = \Delta \Phi_{2,\text{out}} = \sum_{k=1}^{P} \Delta \Phi_{2,k}^1 + \Delta \Phi_{2,k}^{q_k}, \ldots \hspace{1cm} (5)
\]

The average currents of the input and the output are given by

\[
\overline{I_{\text{in}}} = (\Delta \Phi_{1,\text{in}} + \Delta \Phi_{2,\text{in}})/T_c
\]

\[
\overline{I_{\text{out}}} = (\Delta \Phi_{1,\text{out}} + \Delta \Phi_{2,\text{out}})/T_c, \ldots \hspace{1cm} (6)
\]

From Eqs.(3) ~ (6), the following equation is derived:
Here, we assume that the voltages of the capacitors, $V_{C_k}'s$, satisfy $V_{C_k}(sT_c) \simeq V_{C_k}(sT_c + T_c)$ ($s = 1, 2, \ldots$) when $C_1 = \cdots = C_P = C_o = C$ and $C_oR_o \gg T_c$. In this case, the following equation is obtained:

$$\Delta q_{\Phi_1,V_in} = \frac{1}{P-1}C(V_{in} - V_{out}) - CV_{out}, \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots 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When $C_o = 0$, the output voltage ripple $\Delta V_{out}$ is obtained as follows. In the case of $\Phi_1$, the output voltage $V_{out,\Phi_1}(t)$ is given by

$$V_{out,\Phi_1}(t) = \frac{2V_{in}}{3} \exp\left(-\frac{2t}{CR_o}\right), \quad \cdots \cdots \cdots (23)$$

On the other hand, in the case of $\Phi_2$, the output voltage $V_{out,\Phi_2}(t)$ is given by

$$V_{out,\Phi_2}(t) = \left\{ \frac{V_{in}}{2} + \frac{V_{in}}{6} \exp\left(-\frac{2T}{CR_o}\right) \right\} \times \exp\left(-\frac{3t}{2CR_o}\right), \quad \cdots \cdots \cdots (24)$$

Then the output voltage ripple $\Delta V_{out}$ is obtained by

$$\Delta V_{out} = V_{out,\Phi_1}(0) - V_{out,\Phi_2}(T) = \frac{2V_{in}}{3} - \left\{ \frac{V_{in}}{2} + \frac{V_{in}}{6} \exp\left(-\frac{2T}{CR_o}\right) \right\} \times \exp\left(-\frac{3T}{2CR_o}\right), \quad \cdots \cdots \cdots (25)$$

As Fig.8 shows, the equivalent circuit of the proposed converter is the same as that of the conventional converters (3) (4) (13) (14). Therefore, the characteristic behavior of the proposed converter becomes the same as that of the conventional converters. When the output current is 0 and the voltage-drop caused by power-switches is free, the ideal output voltage $V_{out}$ is given by

$$V_{out} = \frac{Q}{P}V_{in},$$

where $Q \leq P$. \cdots \cdots \cdots (26)

Table 1 shows the types of power conversions. As Table 1 shows, the proposed converter can provide various types of stepped-down voltages. Table 2 shows the material cost for the power converters. When $N \leq 3$, the hardware-cost for the proposed converter is smaller than that for the conventional converters. Figure 9 shows the examples of the proposed converters for specific uses. As Fig.9 shows, the number of the power-switches can be reduced by choosing the converter according to applications. For example, when $2/3$ step-down, the number of the power-switches for Fig.9 (c) is below the half of that for the ring-type converter.

### 3. Simulation

To confirm the validity of the circuit design, SPICE simulations were performed concerning the 3-stage power converters shown in Figs.10 ~ 13†. In these

![Fig. 10. 3-stage series-parallel type DC-DC converter](image)

![Fig. 11. 3-stage ring-type DC-DC converter](image)

†The power converters shown in Figs.11 and 12 can provide the output voltage $V_{out} \in \{ (1/2) V_{in}, (1/3) V_{in}, (2/3) V_{in} \}$. The power converter shown in Fig.10 realizes 1/2-step down and 1/3-step down, and the proposed converter of Fig.13 for specific uses provides 2/3-stepped down voltage.

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Table 1. Types of power conversions

<table>
<thead>
<tr>
<th>Type of conversion</th>
<th>Step of conversion</th>
</tr>
</thead>
<tbody>
<tr>
<td>Series-parallel type of Fig.1</td>
<td>Step-up and step-down</td>
</tr>
<tr>
<td>Series-parallel type of Fig.2</td>
<td>Step-down</td>
</tr>
<tr>
<td>Ring type</td>
<td>Step-down and step-down</td>
</tr>
<tr>
<td>Proposed</td>
<td>Step-down</td>
</tr>
</tbody>
</table>

Table 2. Material costs for power converters

<table>
<thead>
<tr>
<th>Power switch</th>
<th>Capacitor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Series-parallel type of Fig.1</td>
<td>$4N - 1$</td>
</tr>
<tr>
<td>Series-parallel type of Fig.2</td>
<td>$3N - 1$</td>
</tr>
<tr>
<td>Ring type</td>
<td>$4N$</td>
</tr>
<tr>
<td>Proposed</td>
<td>$(2N - 1) + 2 \sum_{k=1}^{N-1} (N - k)$</td>
</tr>
</tbody>
</table>

$(N = 2, 3, \ldots)$
simulated converters, B1 denotes the bootstrap circuit shown in Fig.14. To alleviate the threshold voltage drop caused by power-switches, the bootstrap circuits were attached to the power-switches.

Figure 15 shows the transient characteristics of the simulated converters. The SPICE simulations were performed under the conditions that the input voltage $V_{in} = 3.6V$, $C_j = 5\mu F$, $C_o = 5\mu F$, $C_b = 2nF$, and the on-resistance of the power-switch $R_{on} = 0.25\Omega$. In Fig.15, the output load $R_o$ was set to 7Ω. The settling time of the proposed converter is less than 20$\mu$s at 500kHz. As Fig.15 shows, the settling time of the series-parallel type power converter is the longest.

Figure 16 shows the ripple noise for the output capacitor $C_o$. As Fig.16 shows, the ripple noise of the proposed converter and the ring-type converter are smaller than that of the series-parallel type power converter.

Figure 17 show the power efficiency of the simulated converters. The proposed converters and the series-parallel type converter are superior to the ring-type power converter in respect of the power efficiency. In the case of 2/3 step-down conversion, the power efficiency of the proposed converter of Fig.13 is 92.7% in the output current about 320mA.

4. Conclusion

A step-down DC-DC converter with charge-average processes has been proposed in this paper. The validity of the circuit design was confirmed through SPICE simulations. The simulations showed the following results.

1. Different from the series-parallel type power converter, the proposed converter can provide various types...
of output voltages such as \((2/3)V_{in}\), \((3/2)V_{in}\), and so on. 2. When the number of the capacitors is less than 4, the material cost for the proposed converter is smaller than that for the conventional power converters 3. For the input voltage \(3.6\)\(V\), the power efficiency of the proposed converter is \(92.7\) \% in the output current about \(320mA\).

The further improvement of efficiency and the analysis of the proposed circuit containing parasitic elements are left to the future study.

(Manuscript received June 3, 2004, revised Dec. 22, 2004)

References


Fig. 16. Ripple noise for power converters.

Fig. 17. Power efficiency for the simulated converters.
A Step-Down Power Converter with Charge-Average Processes

Fumio Ueno (Member) received the B.E. degree in electrical engineering from Kumamoto University, Japan, in 1955, and the M.E. degree and the D.E. degree from Kyushu University Fukuoka, Japan, in 1964, 1968 respectively. He worked for the faculty of Kumamoto University, where he was a Professor, Dean in 1992. From 1994 to 2001, he was the President at Kumamoto National College of Technology. Now, he works for Sojo University as Dean at Faculty of Computer and Information Sciences, and IEICE Kyushu Branch Chair in 1995. His main interest lies in the field of active networks. Dr. Ueno is a member of IEICE, IEEJ, JSOFT, and IEEE.

Hongbing Zhu (Member) has the B.S., the M.S. and the Ph.D. degrees. He was an Assistant Professor and Lecture of Information Science & Engineering faculty, Wuhan University of Science & Technology, and Information Processing Center, Kumamoto University. And he worked as a visiting scholar at Kyushu Tokai University and Kumamoto University. Now, he is an Associate Professor of Hiroshima Kokusai Gakuen University. His current research interests include neural networks, non Neumann computer and high-speed processing, etc. He is also a member of IEEE, IEICE, JNNS, IPSJ.

Toru Tabata (Non-member) was born in Kumamoto, Japan in 1946. He received the B.E., the M.E., and the Ph.D. degrees. He is an Assistant Professor and Lecture of Information Science & Engineering faculty, Kumamoto University, Kumamoto, Japan, in 1970, 1972, and 1999, respectively. Currently, he is a Professor of the Department of Electronic Control at Kumamoto National College of Technology. His research interests and activities include the multiple-valued computer arithmetic circuits. He is a member of IEICE and IPS of Japan.

Takahiro Inoue (Member) received the B.E. and the M.E. degree from Kumamoto University, Kumamoto, Japan in 1969 and 1971, respectively, and the D.E. degree from Kyushu University, Fukuoka, Japan in 1982. From 1971 to 1974, he worked as a Research Staff at Hitachi, Ltd., Yokohama, Japan. In 1975, he joined the faculty of Kumamoto University, where he is now a Professor. Dr. Inoue’s current research interests include switched-capacitor/switched-current filters, continuous-time IC filters, low-power/low-voltage analog integrated circuits, and analog/digital intelligent circuits and systems. He is a member of the Institute of Electrical and Electronics Engineers and he served as an Associate Editor of Transactions on Fuzzy Systems during 1994-1996. He is also a member of the Japanese Neural Network Society, and the Physical Society of Japan.

Kei Eguchi (Member) received the B.E., the M.E., and the D.E. degrees from Kumamoto University, Kumamoto, Japan in 1994, 1996, and 1999, respectively. Presently he is an Associate Professor in Kumamoto National College of Technology. His research interests include nonlinear dynamical systems, intelligent circuits and systems, and low-voltage analog integrated circuits. He is a member of IEICE.

Shinya Terada (Non-member) received the B.E. and M.E. degree from Sojo University, Kumamoto, Japan in 2002, 2005 respectively. He is now Doctoral course student at Division of Energy Electronics, Sojo University. He is interested in switched-capacitor power electronics circuits. He is student member of IEICE, and IEEE.


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