Synthesis and analysis of a discrete-time CNN using 1-dimensional cell circuits with $S$ stable points ($S = 2, 3, 4, \ldots$)

Member Kei EGUCHI (Kumamoto National College of Technology)
Non-member Yasukazu SEIKI (Kumamoto National College of Technology)
Non-member Toru TABATA (Kumamoto National College of Technology)
Non-member Hongbing ZHU (Hiroshima Kokusai Gakuin University)
Member Fumio UENO (Kumamoto National College of Technology)
Member Takahiro INOUE (Kumamoto University)

In this paper, a discrete-time CNN using 1-dimensional cell circuits with $S$ stable points ($S = 2, 3, 4, \ldots$) is proposed. The circuit structure and the behavior of the proposed CNN is simple by exploiting discrete-time 1-dimensional circuits as the cell circuits. Since the proposed cell circuit takes as much as $S$ states, the proposed CNN can demonstrate the multiple-valued traveling wave phenomena. Furthermore, the proposed cell circuit is suitable for integration thanks to the circuit design by using switched-current (SI) techniques. The computer simulations are performed concerning a 2-dimensional CNN which is constructed with the proposed cell circuits. The 1-dimensional cell circuit with $S$ stable points is designed by a standard CMOS process. Furthermore, the proposed cell circuit is built with commercially-available IC's. The experimental result is in close agreement with the simulation result. The proposed CNN is integrable by a standard CMOS technology.

Keywords: cellular neural networks, traveling waves, switched current, discrete-time circuits, analog circuits

1. Introduction

Recently, the CNNs (Cellular Neural Networks) using chaos circuits attract many researchers' attention. In these CNN, traveling waves can be observed. The traveling wave is one of the most frequently encountered phenomena in the study of natural phenomena in physics and biology [1],[2]. The CNN using chaos circuits opens up new vistas for application systems, for example, models for the transport phenomena in biological and physical systems, shortest-path finding systems, and so on [1]-[7]. For this reason, many researcher's have shown prototypes of the CNN using chaos circuits [3]-[5]. These CNNs exploit Chua's chaos circuits [8]-[10] as the cell circuits. Since the cell circuits used in these CNNs have two stable points, $P_-$ and $P_+$, the CNNs employing Chua's chaos circuits can demonstrate binary-valued traveling wave phenomena. However, the circuit structure and the chaotic behavior of Chua's circuit are very complicated since it is a 3-dimensional continuous-time chaos circuit. In the design of the CNNs, the simplicity of the behavior as well as the circuit structure are important. Being distinct from such features, hardware-implementation of the CNN with a standard IC technology is favorable. This feature will enable the CNNs to get into experimental tools for the large scale networks.

In this paper, a discrete-time CNN using 1-dimensional cell circuits with $S$ stable points ($S = 2, 3, 4, \ldots$) is proposed. The circuit structure and the behavior of the proposed CNN is simple by exploiting discrete-time 1-dimensional circuits as the cell circuits. The proposed CNN can demonstrate the multiple-valued traveling wave phenomena since the proposed cell circuit takes as much as $S$ states. Furthermore, the proposed cell circuit synthesized using switched-current (SI) techniques [11],[12] is suitable for integration since 1. SI circuits can be implemented by a standard digital process, 2. they exhibit low sensitivity to both temperature variations and supply voltage variations, and 3. they are more robust than voltage-mode counterparts against the reduction of the supply voltages.

Fig. 1 Circuit architecture of the discrete-time CNN which consists of 1-dimensional cell circuits with $S$ stable points ($S = 2, 3, 4, \ldots$).
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The computer simulations are performed concerning a 2-dimensional CNN which is constructed with the proposed cell circuits. Furthermore, the proposed cell circuit is built with commercially-available IC's.

2. Architecture

Figure 1 shows the circuit architecture of the proposed CNN. The proposed CNN consists of $a \times b$ cells. In Fig. 1, $D_{i,j}$ is a non-negative diffusion coefficient. The dynamics of the proposed CNN is based on the following equation:

$$X_{i,j}(t+1) = FC(X_{i,j}(t))$$

$$= F(X_{i,j}(t)) + Q, \quad \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots (1)$$

where

$$Q = D_{i,j-1}(t_a) X_{i-1,j}(t) + D_{i,j+1}(t_a) X_{i+1,j}(t)$$

$$+ D_{i-1,j}(t_a) X_{i-1,j}(t) + D_{i+1,j}(t_a) X_{i+1,j}(t)$$

and

$$D_{i,j}(t_d) = \begin{cases} D_{i,j} & \text{if } t_d = q_t, \\ 0 & \text{if } t_d \neq q_t. \end{cases}$$

In Eq.(1), $X_{i,j}(t)$ is a positive variable, $F(\cdot)$ and $FC(\cdot)$ are piecewise-linear functions which have $S$ stable points ($S = 2, 3, 4, \ldots$), $D_{i,j}$ is a positive constant, and $q$ is an integer parameter. Figure 2 shows an example of the nonlinear function when $t_d \neq q_t$. The nonlinear function $F(\cdot)$ in Eq.(1) is given by the following condition:

$$F(X) = F_0(X) + F_1(X) + \ldots F_S(X)$$

$$\left( X \in [T_0, F_S^{-1}(T_S) ) \right), \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots (2)$$

where $F_n(X)$ ($n = 0, 1, \ldots, S$) is the linear function on the interval $[T_n, T_{n+1}]$. The linear function $F_n(X)$ satisfies the following conditions:

$$T_0 = 0 \quad \text{and} \quad T_{S+1} = F_S^{-1}(T_S)$$

and $F_n(T_n) < T_{n+1}$

and $\frac{dF_n(X)}{dX} < 1$. \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots (3)$

In Fig. 2, $P_0$ is an unstable point and $P_k$'s ($k = 1, \ldots, S$) are stable points. The stable point, $P_k$ ($k = 1, \ldots, S$), satisfies the following condition:

$$P_k = FC(P_k) \quad (k = 1, \ldots, S). \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots (4)$$

When the nonlinear function satisfies

$$FC(T_k) < T_{k+1}, \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots (5)$$

the basin $[5],[6]$ of the stable point $P_k$ ($k = 1, \ldots, S$) is given by the following equations:

$$B(P_1) = (0, T_2),$$

$$B(P_2) = (T_2, T_3),$$

$$\ldots$$

$$B(P_S) = (T_S, T_{S+1}). \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots (6)$$

These equations mean that the state of the $i,j$-th cell will settle down to $P_k$ when $X \in [T_k, T_{k+1}]$. When $t_d \neq q_t$, the state of the cell cannot transfer to the other states since the nonlinear function satisfies the conditions of Eqs.(3) and (5) (see Fig.3 (a)). On the
other hand, the state of the cell can transfer from $P_k$ to the higher state (see Fig.3 (b)) when

$$t_d = q_t$$
and
$$F_k(T_k) + Q < T_{s+1}$$
and
$$F_k(T_k) + Q > T_{s+1}.$$  (7)

The parameter $Q$ for the $i,j$-th cell is determined by the diffusion coefficient $D_{i,j}(t_d)$ and the states of the neighbor cells, $X_{i-1,j}(t)$, $X_{i+1,j}(t)$, $X_{i,j-1}(t)$, and $X_{i,j+1}(t)$. From Eqs.(6) and (7), the proposed cell can take as much as $S$ of states. After the state of the cell transferred from $P_k$ to the higher state, the state of the cell settles down to around $P_l$ ($l > k$) by closing the connection of the cell (see Fig.3 (c)). When $t_d \neq q_t$, the variable $X_{i,j}(t)$ is mapped $q-1$ times by FC. Hence, the state of the cell is affected by the parameter $q$.

The validity of the circuit algorithm will be confirmed in Sect.4.

3. Circuit Structure

Figure 4 shows the proposed cell circuit designed by using SI techniques. The synthesis of this circuit is based on the following equation:

$$X_{i,j}(t+1) = I_3 - [(I_1 \oplus L_1 X_{i,j}(t)) + (X_{i,j}(t)/L_2 \oplus I_2)]$$
$$+ u(X_{i,j}(t) - I_3) \cdot H_2 + \cdots + u(X_{i,j}(t) - I_S) \cdot H_S$$
$$+ D_{i,j}(t_d) X_{i,j-1}(t) + D_{i,j+1}(t_d) X_{i,j+1}(t)$$
$$+ D_{i-1,j}(t_d) X_{i-1,j}(t) + D_{i+1,j}(t_d) X_{i+1,j}(t).$$  (8)

where $u(\cdot)$ is the unit step function and $\oplus$ is the bounded-difference operator defined as

$$\alpha \oplus \beta \triangleq \begin{cases} \alpha - \beta & (\alpha > \beta), \\ 0 & (\alpha \leq \beta). \end{cases}$$  (9)

Different from the circuit proposed in [11], the proposed cell has $S$ stable points and cannot generate chaotic signals without the effect of the other cells. In Fig.4, the operations, $(I_1 \oplus L_1 X(t))$ and $(X(t)/L_2 \oplus I_2)$, are realized by the bounded-difference circuits composed of the current mirrors and the diode-connected MOSFET's. The parameters, $L_1$ and $L_2$, are realized by the current-copying ratios in the bounded-difference circuits. The operation, $u(\cdot)$, is realized by the current comparator composed of the CMOS inverters and the current mirrors. The delay block is the SI track & hold circuit [11]. In the delay block, the diffusion coefficients, $D_{i,j}$'s, are realized by the current-copying ratios. By setting the gate bias $\phi_{d_{i,j}}$ to 0, the proposed SI cell circuit can close the connection of the $i,j$-th cell. Therefore, $\phi_{d_{i,j}} = 0$ corresponds to $D_{i,j}(t_d) = 0$. The output of the operation block is delayed by one cycle and it is fed back to the input terminal of the operation block. The initial value $X_{i,j}(0)$ of this circuit is given by $V_{in}$ in the delay block. The operations of the switches, $\phi$, $\phi'$, and $\phi_{d_{i,j}}$, are set to as shown in Fig.4. Here, the period of $\phi_{d_{i,j}}$ corresponds to the parameter $q$.

4. Simulation

To confirm the validity of the circuit design, numerical simulations are performed regarding to the circuit algorithm. The dynamics of the simulated CNN is based on the following equations:

$$X_{i,j}(t+1) =$$

Fig.5 Nonlinear function of the proposed cell obtained by numerical simulation.

Fig.4 SI cell circuit with $S$ stable points ($S=1, 2, 3, \ldots$).

1 As Fig.3 (b) shows, the state of the cell transfers to the higher state since the position of the stable point $P_k$ is moved by the effect of the other cells, $Q$.

11 From Eqs.(11) ~ (3), the state of the $i,j$-th cell settles down around $P_l$ ($l > k$) by setting $q \geq 1$. 2001
The proposed cell in the simulated CNN has three stable points. Hence, the proposed cell in the simulated CNN has as much as three states. The basin of the stable point, $P_k$ ($k = 1, \ldots, 3$), is given by the following equations:

$$B(P_1) = (0, 0.55).$$

$$B(P_2) = [0.55, 1.05).$$

$$B(P_3) = [1.05, 55.5).........(11)$$

In the numerical simulations, the parameter $q$ for $\phi_{d_{i,j}}$ (see in Fig.4) was set to 5.

Figure 5 shows the simulated nonlinear function of the proposed cell. Figure 6 shows the traveling wave in a $8 \times 8$ array of the proposed cells. In Fig.6, the hatched cells are the obstacles created by setting the diffusion coefficients to 0. The diffusion coefficients of the non-hatched cells, $D_{i,j}$'s, were set to 0.02. In Fig.6, the Goal cell has switched from $P_1$ to $P_3$ after 115 cycles. Figure 7 shows the traveling wave in a $16 \times 16$ array of the proposed cells. In numerical simulations...
of Fig. 7, the diffusion coefficients of all cells were set to 0.02. As Fig. 7 shows, the multiple-valued traveling wave phenomena such as a ripple mark can be modeled by the proposed CNN.

In Figs. 6 and 7, the characteristics of the proposed CNN were analyzed by numerical simulations. However, the non-ideal effects of the circuit implementation such as the clock feedthrough, finite output resistance of the transistors, etc. cannot be analyzed by this method. Therefore, to analyze those non-ideal effects and to confirm the validity of the above-mentioned simplification, the SPICE simulations [13] are performed regarding to a 4 × 4 array of the proposed cell circuits. To save space, only the SPICE simulation results concerning the proposed cell circuit with two stable points will be given. The proposed cell circuit is designed by assuming a standard CMOS process.

Figure 8 shows the SI cell circuit used in SPICE simulations. SPICE simulations were performed under the conditions that $V_{dd} = 5V$, $I_1 = 6\mu A$, $I_2 = 0.4\mu A$, $I_3 = 6\mu A$, $I_{F_2} = 6\mu A$, $I_{F_2} = 6\mu A$, $L_1 = 6$, $L_2 = 4$, and $D_{i,j} = 1/3$. Figure 9 shows the simulated nonlinear function of the cell circuit. The nonlinear function of this circuit has two stable points. The basin of the stable point, $P_k$ ($k = 1, 2$), is given by

$$B(P_1) = (0\mu A, 6\mu A)$$

$$B(P_2) = (6\mu A, 30\mu A)$$

Figure 10 shows the traveling wave in a 4 × 4 array of the proposed cell circuits. In the SPICE simulation of Fig. 10, the initial state of the 1st cell was set to $P_2$ and the initial states of all the other cells were set to $P_1$. 

![Fig. 10 Simulated traveling wave in a 4 × 4 array. (a) t = 20ms. (b) t = 40ms. (c) t = 70ms. (d) t = 100ms.](image-url)
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In Fig. 10, the hatched cells are the obstacles created by setting \( \phi_{di,j} \) to 0 V. The parameter \( \phi_{di,j} \) of the non-hatched cell was set to 5 V. Thus, the proposed circuit can control the initial state of the CNN, electronically. Figure 11 shows the states of the cell circuits obtained by the SPICE simulations. From Figs. 10 and 11, the traveling wave has propagated to the 16th cell after 100 \( \mu \)s.

5. Experiment

To analyze the non-ideal effects of the proposed cell circuit, the experiments concerning the nonlinear function and the state of the cell circuit are performed regarding to the experimental circuit. The experimental circuit was built with commercially available IC's 4007UB and 4528B, and discrete bipolar transistors, 2SC1815 and 2SA1085. The IC's 4528B were used to generate the clock pulses, \( \phi \) and \( \tilde{\phi} \), in the delay block. The discrete bipolar transistors were used to realize the current sources. And the value of the capacitor \( C \) was set to 10 nF.

Figure 12 shows the nonlinear function of the experimental circuit. Figure 12 is in close agreement with the simulated result in Fig. 9. Figure 13 shows the state of the proposed cell in the experimental circuit.

In Fig. 10, the cell circuit used in SPICE simulations has 2 stable points, the parameter \( \phi_{di,j} \) of the non-hatched cell was fixed to 5 V.

6. Discussion

In the past, several types of CNNs using chaos circuits have been proposed. Among others, V. Pérez-Munuzuri et al. adopted Chua's chaos circuit to realize CNN using chaos circuit [5],[6]. This CNN employing Chua's chaos circuits can demonstrate binary-valued traveling wave phenomena. The cell circuit of this CNN is a 3-dimensional continuous-time chaos circuit designed by voltage-mode techniques.

On the other hand, the advantages of the proposed method are as follows: 1. The circuit structure and the behavior of the proposed CNN is simple by exploiting discrete-time 1-dimensional circuits as the cell circuits. 2. Since the proposed cell circuit takes as much as \( S \) of states, the proposed CNN can demonstrate the multiple-valued traveling wave phenomena. 3. The proposed cell circuit synthesized using switched-current (SI) techniques is suitable for integration since a) SI circuits can be implemented by a standard digital process, b) they exhibit low sensitivity to both temperature variations and supply voltage variations, and c) they are more robust than voltage-mode counterparts against the reduction of the supply voltages.

Table 1 shows the comparison of the above mentioned methods.

7. Conclusion

A discrete-time CNN using 1-dimensional cell circuits with \( S \) stable points \( (S = 2, 3, 4, \ldots) \) has been proposed in this paper.

The numerical simulations showed that the proposed CNN can demonstrate the multiple-valued traveling
wave phenomena. The SPICE simulations concerning a 4 × 4 array of the proposed cell circuits showed that the proposed CNN can search the shortest-path after 100 μs. The experiment of the breadboard circuit was in close agreement with the simulation result. The proposed CNN is integrable by a standard CMOS technology.

(Manuscript received Dec. 17, 1999, revised Nov. 27, 2000)

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Kei Eguchi (Member) was born in Saga, Japan in 1972. He received the B.E., the M.E., and the D.E. degrees from Kumamoto University, Kumamoto, Japan in 1994, 1996, and 1999, respectively. Presently he is a lecturer in Kumamoto National College of Technology. His research interests include nonlinear dynamical systems, intelligent circuits and systems, and low-voltage analog integrated circuits. He is a member of IEICE.

Yasukazu SEIKI (Non-member) received the B.S., M.S. degrees in Engineering from the University of Yamaguchi in 1986 and 1988, respectively. He worked for the University of Nagasaki from 1968 to 1988. Presently, he is an associate professor at the Department of Computer Science and Technology, Kumamoto National College of Technology. His research interests include agent-oriented circuit design, FPGA design for intelligent circuits, and applications of chaos circuits.

Toru Tabata (Non-member) was born in Kumamoto, Japan in 1946. He received the B.E., the M.E., and the D.E. degree in electrical engineering from Kumamoto University, Kumamoto, Japan, in 1970, 1972, and 1999, respectively. Currently, he is a Professor of the Department of Electronic Control at Kumamoto National College of Technology. His research interests and activities include the multiple-valued computer arithmetic circuits.

Hongbing ZHU (Non-member) received the B.S. and M.S. degrees in Electrical Engineering & Computer Science, from Wuhan Yijin University, Wuhan, P. R. of China, in 1982 and 1988, respectively. From 1982 to 1991 he was an Assistant and Lecturer of Wuhan Yijin University of Science and Technology. He worked as a visiting scholar at Kyushu Tokai University, Japan and Kumamoto University, Japan in 1991 and 1992, respectively. He obtained a Ph.D. degree from Kumamoto University, in 1996. He is now a lecturer of Hiroshima Kokusai Gakuin University, Japan. His research interests include neural networks and high-speed processing, etc.

Fumio UENO (Member) received the B.E. degree in electrical engineering from Kumamoto University, Kumamoto, Japan, in 1955, and M.E. degree and D.E. degree from Kyusyu University, Fukuoka, Japan, in 1964, 1968 respectively. He was the faculty of Kumamoto University, where he was a Professor, Dean in 1992. Since 1994 he has been the President at Kumamoto National College of Technology, and IEICE Kyusyu Branch Chair in 1995. His main interest lies in the field of active networks.

Takahiro Inoue (Member) received the B.E. degree in electrical engineering from Kumamoto University, Kumamoto, Japan, in 1955, and M.E. degree and D.E. degree from Kyusyu University, Fukuoka, Japan in 1964, 1968 respectively. He was the faculty of Kumamoto University, where he was a Professor, Dean in 1992. Since 1994 he has been the President at Kumamoto National College of Technology, and IEICE Kyusyu Branch Chair in 1995. His main interest lies in the field of active networks.

Takahiro Inoue (Member) received the B.E. degree and the M.E. degree from Kumamoto University, Kumamoto, Japan in 1969 and 1971, respectively, and the D.E. degree from Kyusyu University, Fukuoka, Japan in 1982. From 1971 to 1974, he worked as a Research Staff at Hitachi, Ltd., Yokohama, Japan. In 1975, he joined the faculty of Kumamoto University, where he is now a Professor. Dr. Inoue’s current research interests include switched-capacitor/switched-current filters, continuous-time IC filters, low-power/low-voltage analog integrated circuits, and analog/digital intelligent circuits and systems.