New Methods for the Active Compensation of Unbalanced Supply Voltages for Two-Stage Direct Power Converters

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Unbalanced supply voltages can be fully compensated in boost type power converters with active front end if sufficient energy storage is provided by the DC-link capacitor. In converters that have no energy storage, matrix converters for example, the maximum voltage transfer ratio will be reduced if one or more input lines are at a reduced voltage. Traditional control techniques (passive compensation methods) compensate the effect of unbalanced voltage supply for matrix converters but limit the output voltage/powe depending on the unbalance level.

This paper proposes two methods to actively (no loss in output voltage capability) compensate the effect of unbalanced voltage supply: the first one shown in Fig. 1(a), utilizes the clamp capacitor, which is normally needed to protect a Direct Power Converter (DPC), to extend the operating range of a Two-Stage DPC during unbalanced supply conditions preserving its theoretic maximum voltage transfer ratio capability; the second one shown in Fig. 1(b) is a new topology based on a hybrid approach, consisting of an H-bridge inverter inserted into the dc-link, which is also able to preserve the output voltage capability under unbalanced supply conditions. Both solutions are validated through simulations.

Unbalanced voltage supply cause the input voltage vector locus to become an ellipse, which means that the average over a switching period of the rectified voltage to vary in a much wider range than in the ideal case (sinusoidal and balanced supply voltages). The principle of active compensation is to use energy storage in order to store energy when the rectified voltage is high (positive and negative voltage sequences point in the same direction) which would be used when this is low (the positive and negative sequences point opposite). Fig. 2(a) shows the DC-link voltage seen at the inversion stage terminals when there is no active compensation and the average dc-link voltage reaches a minimum of 440 V, which means that the voltage transfer ratio defined as a ratio between the output voltage divided to the direct sequence of the input voltage is decreased from 0.866 (ideal case) to 0.78. By applying active compensation using the clamp circuit, this is restored back to 0.866 as shown in Fig. 2(b). The price to be paid for improving the converter robustness against grid disturbances is a slightly oversized clamp capacitor, the need to introduce an extra IGBT in the clamp circuit and the degradation of input current quality due to uncontrolled capacitor charging, which is shown in the full paper.

Active compensation using an hybrid approach is not only able to restore the voltage transfer ratio, but also stabilizes the average over a switching period and boost its value to a corresponding voltage transfer ratio of 0.909, which means that the voltage delivered to the output side falls within the normal voltage tolerance (±10%) of a motor which will allow this topology to directly compete the well established back-to-back voltage source converters.
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Unbalanced supply voltages can be fully compensated in boost type power converters with active front end if sufficient energy storage is provided by the DC-link capacitor. In converters that have no energy storage, for example in a matrix converter, the maximum voltage transfer ratio will be limited if one or more input lines is at a reduced voltage. Control techniques to compensate the effect of unbalanced voltage supply for matrix converters allow for a limited output voltage and power capabilities, which depends on the level of unbalance. This paper proposes the utilization of the clamp capacitor, which is normally needed to protect a Direct Power Converter (DPC), to extend the operating range of a Two Stage DPC during unbalanced supply conditions preserving its theoretic maximum voltage transfer ratio capability. A new topology based on a hybrid approach, consisting of an H-bridge inverter inserted into the intermediary link, which is also able to preserve the output voltage capability under unbalanced supply conditions, is proposed. Both solutions are validated through simulations.

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1. Introduction

Currently, the most successful converter topology used in Adjustable Speed Drives (ASDs) consists of a diode bridge rectifier supplying a Voltage Source Inverter (VSI) via a high storage capacitor bank. It has the advantage of being very simple and cheap but as the installed power in ASDs increases, negative effects on the mains (current distortion, EMI) have been observed\(^1\). These shortcomings, in conjunction with the lack of robustness against unbalanced supply voltage require the use of controlled active front-end stages in future ASDs. The back-to-back Voltage Source Inverter features a fully controlled active front-end rectifier that solves all previously presented problems while requiring the lowest amount of switching devices (6 IGBTs and diodes) but the installed energy in passive components (boost inductances) remains high. The reduction of the DC-link capacitor has been investigated but film capacitors, which have lower energy density, are needed due to the larger current ripple, which low size electrolytic capacitors cannot cope with. However, in order to provide balanced input currents while operating with unbalanced supply and having reduced energy storage in the DC-link will result in larger DC-link voltage ripple due to the power ripple caused by the inverse sequence voltage component. In order to avoid overmodulation of the PWM rectifier, it is necessary to limit the DC-link voltage to the peak value of the line-to-line input voltage, which means that the whole converter will be subject to high voltage stress: oversized component (semiconductor and DC-link capacitor) and switching losses.

An alternative to this is the direct power conversion (DPC) approach with forced commutated semiconductor devices (IGBTs, GTOs, etc). The matrix converter\(^2\)–\(^8\), which is the most known DPC representative, has challenged the research in the last 25 years due to the many unsolved implementation aspects, which were solved lately but implies a higher cost. Another possibility to implement DPC providing similar input and output performance as a standard single-stage matrix converter is the two-stage DPC\(^9\)–\(^13\), also referred in the literature as “indirect MC”, “dual bridge MC” or “sparse matrix converter” which consists of a current source type rectifier stage directly linked to a voltage source type inverter stage. It has been shown already that this two-stage DPC allows for reducing the number of IGBTs\(^12\), much simpler commutation of the switches compared to a single-stage matrix converter\(^11\), possibility to build more complex converter structures with multiple supply and load ports\(^13\).

Unbalanced voltage supply can be fully compensated in boost type power converters with active front end where enough energy storage is installed in the DC-link capacitor. In DPCs, which have no energy storage (e.g. matrix converter), it is expected that the converter output voltage capability will be affected. Control techniques to compensate the effect of unbalanced voltage supply for matrix converters\(^14\)–\(^17\) allow for a limited output voltage and power capabilities, which depends on the level of unbalance. This is illustrated in Fig. 1, where the input voltage locus, the hexagon of the output voltage vectors and the output voltage locus are shown in three situations: balanced input voltages (Fig. 1(a)), unbalanced voltage supply with the best case position of inverse sequence in respect to the hexagon (tangent to ellipse in four points (Fig. 1(b)) and the worst case situation where the hexagon is tangent to the ellipse in only two
2. Two-Stage DPC Topology with A Clamp Circuit

In Ref. (3), (4), (7), (8) has been shown that a clamp circuit is needed to allow safe shutdown of a DPC that supplies an inductive load, while the size of the clamp capacitor depends on the amount of magnetic energy stored in the load inductance. Normally, the clamp circuit consists of a three-phase diode bridge connected to the load terminals on the AC side and to the clamp capacitor on the dc-side. This clamp circuit is also needed on the input side in order to protect the DPC from possible grid disturbances. Therefore, in most of the applications, it consists of twelve diodes and a capacitor. In Ref. (17) it has been proposed to use an IGBT connected in anti-parallel to the clamp capacitor diode to allow circulation of the magnetic load energy when the power factor is poor, because that application utilized a unidirectional rectification stage.

As in this case the objective is to increase the output voltage capability during unbalanced voltage supply, the utilization of clamp capacitor to store a certain amount of energy is desired. The equivalent scheme of the topology shown in Fig. 2, when the clamp capacitor IGBT is off/on is shown in Fig. 3. When the IGBT is off, the converter topology is equivalent to the standard 2-stage DPC (Fig. 3(a)), and this will be used when operating in the region where the inverse sequence cause the increase of the magnitude of the input voltage vector. During this period, the clamp capacitor will charged to the maximum available voltage level. When the input voltage vector magnitude decreases below the desired output voltage level, it is necessary to utilize also the clamp capacitor voltage to boost up the average value of the dc-link voltage seen by the inversion stage. Therefore, the equivalent scheme of that switching sequence becomes as shown in Fig. 3(b).

3. Space Vector Modulation for A Two-Stage DPC

In Ref. (11), it has been shown that the implementation of Space Vector Modulation (SVM) for a two-stage DPC is identical to the case of a matrix converter controlled by an indirect SVM (5), therefore only the final equations are presented here. SVM produces a combination of two adjacent active vectors and a zero-vector to synthesize a reference vector of variable amplitude and angle. The proportion between the duty-cycles of the two adjacent vectors gives the direction and the duty-cycle of the zero-vector determines the magnitude of the reference vector. The input current vector \( I_{in} \) (only its angle) is the reference of the rectification stage (Fig. 4(a)) and the output voltage vector \( V_{out} \) is the reference of the inversion stage (Fig. 4(b)). The duty-cycles of the active switching vectors for the rectification stage, \( \text{V}_{\alpha}, \text{V}_{\beta} \) are given by (1) and the duty-cycles of active switching vectors for the inversion stage, \( \text{V}_{\alpha1}, \text{V}_{\beta1} \) are given by (2).

In the rectification stage, the zero-vector is eliminated and the switching sequence consists only of the two adjacent current vectors (line-to-line voltages). The zero-vector is applied by the inversion stage according to its need.

\[
d_{\gamma} = m_1 \cdot \sin \left( \pi / 3 - \theta_{in} \right) \quad d_{\delta} = m_1 \cdot \sin \theta_{in} \quad \ldots \ldots \quad (1)
\]
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Fig. 3. Equivalent scheme of the two-stage DPC when: (a) the transistor in the clamp circuit is OFF and the rectification stage is operated in normal DPC mode; (b) the rectification stage is turned OFF and the transistor in the clamp circuit is turned ON (Voltage Source Inverter mode)

Fig. 4. Generation of the reference vectors in a two-stage Direct Power Converter using SVM: (a) rectification stage; (b) inversion stage

d_α = m_U \cdot \sin \left( \frac{\pi}{3} - \theta^*_\text{out} \right) \quad d_β = m_U \cdot \sin \theta^*_\text{out} \quad \cdots (2)

where \( m_I \) and \( m_U \) are the rectification and inversion stage modulation indexes, \( \theta^*_\text{in} \) and \( \theta^*_\text{out} \) are the angles within their respective sectors of the input current and output voltage reference vectors.

By using (1), the adjusted rectification stage duty-cycles are found (3), where the modulation index of the rectification stage used in (1) is now unity. These duty-cycles multiply with the switching period and the resulting ON-times directly drive the rectification stage switches. Since the average voltage in the DC-link is not constant anymore due to the cancellation of the zero-vector in the rectification stage, it is necessary to calculate its value to compensate the modulation index of the inversion stage:

\[ V_{PN-avg} = d_β \cdot V_{line-γ} + d_γ \cdot V_{line-δ} \quad \cdots (4) \]

\[ m_U = \sqrt{2} \cdot \frac{V_{out}}{V_{PN-avg}} \quad \cdots (5) \]

The inverter stage may use a double-sided asymmetric PWM switching sequence \( 0_{Y} - α_{γ} - β_{Y+δ} - δ_{0} - 0_{α} \), but with unequal sides because each side corresponds to a rectification switching sequence which has a different DC-link voltage. Therefore, the value of the modulation index \( m_I \) in (2) has to be corrected with the momentary average DC-link voltage \( V_{PN-avg} \) (4), which takes into account its variation. The inversion stage duty-cycles are given in (6):

\[ d_{βγ} = d_γ \cdot \left[ 1 - \left( d_γ + d_δ \right) \cdot \left( d_α + d_β \right) \right] \quad d_{αγ} = d_γ \cdot d_α \]

4. Utilization of the Clamp Capacitor Voltage to Compensate the Effect of Unbalanced Supply

The illustration of the voltage transfer limitation is given in Fig. 5, where the three phase voltages (top side) and the dc-link instantaneous voltage and its average (bottom side) are shown in two situations: balanced supply voltage (Fig. 5(a)) and 10% unbalanced supply voltage (Fig. 5(b)). It is therefore clear that the output voltage generation capability is decreased when the dc-link average voltage reaches minimum and that in the case of unbalanced supply, this is further decreased.

Compensation of unbalanced voltage supply consist first in mixing the two line to line voltages in order to provide a constant average DC-link voltage and its average value into a two-stage DPC presented in two situations: (a) balanced and (b) 10% unbalanced voltage supply, showing where the voltage transfer ratio is limited: (a) 480 V and (b) 450 V

\[ d_{βγ+δ} = (d_γ + d_δ) \cdot d_β \quad d_{αδ} = d_δ \cdot d_α \quad \cdots (6) \]
1.57 J.

In case of 10% unbalance, it can be easily concluded that the clamp capacitor will be connected to the inverter terminals for less than 27% of the switching period, which is the maximum. In case we assume a triangular shape of $d_{clamp}$:

$$
\Delta W_{clamp} = \int d_{clamp}(t) \cdot V_{clamp} \cdot I_{dc\text{-avg}} \cdot dt = 0.5 \cdot d_{clamp\text{-max}} \cdot V_{clamp} \cdot I_{dc\text{-avg}} \cdot \Delta t
$$

In case of 10% unbalance, the time duration where the average dc-link voltage is below the target value is 2 ms, which means that for a 4 kW drive (4.5 kW active power fed to the motor) with 485 V average dc-link voltage and 9.3 A average dc-link current, it will be necessary to store an amount of 1.57 J.
We assumed that the voltage in the clamp circuit would remain constant. Normally, the ripple in the dc-link voltage will vary from (13) which means 625 V when the negative sequence points into the same direction as the direct sequence and the clamp capacitor is fully charged, to (14)

\[
V_{\text{clamp-max}} = (1 + \text{unbal}) \cdot \sqrt{2} \cdot V_{\text{line}} \tag{13}
\]

\[
V_{\text{clamp-min}} = (1 - \text{unbal}) \cdot \sqrt{2} \cdot \frac{\sqrt{3}}{2} \cdot V_{\text{line}} \tag{14}
\]

which means 440 V, when the negative sequence points opposite to the direct sequence. If we assume that we can allow a discharge of the clamp circuit with 50 V, it results a minimum value for the clamp capacitor, which is feasible:

\[
C_{\text{clamp}} = \frac{\Delta W_{\text{clamp}}}{V_{\text{clamp-av}} \cdot \Delta V_{\text{clamp}}} = \frac{1.57}{600 \cdot 50} = 52.3 \mu F
\tag{15}
\]

It is necessary to evaluate the amount of distortion caused by the uncontrolled charging of the clamp capacitor. In order to estimate that, we assume that a three-phase diode rectifier that feeds a dc-link capacitor of same size as the clamp capacitor, selects the highest in magnitude line-to-line input voltage:

\[
I_{\text{clamp-max}} = C_{\text{clamp}} \cdot \frac{dV_{\text{line-in}}}{dt} = 100\pi \cdot C_{\text{clamp}} \cdot (1 + \text{unbal}) \cdot \sqrt{2} \cdot V_{\text{line}} \cdot \sin \left(\frac{\pi}{2} + \alpha_{\text{chg}}\right)
\tag{16}
\]

The worst-case condition takes place when the clamp capacitor is fully discharged to the level given by (14), which gives the corresponding angle for the clamp diode to enter conduction:

\[
\alpha_{\text{chg-min}} = \sin^{-1} \left(\frac{V_{\text{clamp-min}}}{V_{\text{clamp-max}}}\right)
\tag{17}
\]

In case of 10% voltage unbalance, it means that in the worst case condition \(\alpha_{\text{chg}} = \sin^{-1}(440/625) = 0.25\pi\), which in the case of having a 52.5 \(\mu F\) clamp capacitor gives a maximum current peak of 7.3 A. In the case considered in (15) which was used to size the clamp capacitor, the capacitor is discharged only by 50 V giving therefore a higher angle \(\alpha_{\text{chg}} = \sin^{-1}(575/625) = 0.37\pi\), which leads to a smaller charging current peak of only 4 A. This situation is reasonable compared with the input current drawn by the converter when operating at full load (approx 10 A\text{pk}), which proves that this current peaks will not damage the converter, limiting also the input current distortion.

5. The Hybrid Approach

In order to overcome the distortion of the input currents caused by the uncontrolled charging of the clamp capacitor, a hybrid topology has been proposed and investigated. It consists of introducing a variable voltage supply in the intermediary link of the two-stage DPC, in series with the main current path as it is shown in Fig. 7. The purpose of the auxiliary voltage supply is to cover the deficit of voltage, which is characteristic to the two-stage DPC. It is possible to fully compensate the voltage transfer ratio drawback by supplying the missing power to this auxiliary voltage supply, which has a much smaller voltage capability (device voltage rating/install power) than the main DPC. In case it is desired to keep the complexity of the converter low, the increase in the voltage transfer ratio is limited below unity by the condition that the power balance over a cycle of the input voltage to be zero.

The easiest way to implement a variable voltage supply and to achieve high conversion efficiency, which is essential in this kind of application, is by using a PWM H-bridge inverter. The resulting topology is shown in Fig. 8. Its dc-link capacitor provides the energy buffer needed to temporarily compensate the lack of output voltage capability, while its voltage generation capability is given by the difference between unity and the maximum voltage transfer ratio (0.866). As an H-bridge inverter has normally the capability to produce bipolar voltages, it means that its voltage rating is expected to be between 7 and 14% of the main converter devices.

In a two-stage DPC, where the rectifier is controlled by SVM, usually the zero voltage vectors of the converter are produced only by the inversion stage. This allows the reduction of the number of commutation of the rectifier stage, which then reflects in a variable dc-link voltage when calculated over a switching period. This is illustrated in Fig. 5, where the input phase voltages (upper plots) and the instantaneous dc-link voltage and its averaged value over a switching period (bottom) are shown in two situations: balanced (Fig. 5(a)) and 10% unbalanced voltage supply. It is seen that the average dc-link voltage is maximum when the input current vector is near the sector boundary (\(\theta_{\text{in}} = 0 \text{ or } \pi/3\)) and minimum when the reference angle is in the middle of the sector (\(\theta_{\text{in}} = \pi/6\)). In case the angle of the input current reference vector is the same as the angle of the input voltage vector, the maximum of the dc-link voltage will correspond to the peak line-to-line input voltage, while the
minimum \( \theta_{in} = \pi/6 \) will correspond to 0.866 of the peak line-to-line voltage. When the average voltage delivered by the rectifier is too small, it is possible to add a fraction of the voltage available in the H-bridge capacitor by switching the appropriate transistors, introducing the capacitor into the dc-link with its voltage pointing the same direction as the voltage delivered by the rectifier. If the power circulates from the grid to the load, the H-bridge capacitor is discharging. When the average voltage delivered by the rectifier is too high it is possible to subtract a fraction by switching the H-bridge accordingly in order to insert its capacitor in series with the dc-link, having its voltage pointing in opposite direction to the voltage delivered by the rectifier. If the power circulates from grid to the load, it is therefore possible to recharge the H-bridge capacitor. The final effect is that by circulating energy from the H-bridge inverter, which is connected between the rectifier and the inversion stages, it is possible to increase the minimum average dc-link voltage, which is seen by the inversion stage, and therefore to improve the voltage transfer ratio. The same principle may be applied to compensate the negative influence of unbalance on the voltage transfer ratio, which will be exemplified by simulations later.

The amount of voltage produced by the H-bridge can be adjusted from \(-V_C\) to \(+V_C\) by alternating one non-zero voltage switching state and a zero voltage state. The way the hybrid converter changes its switching state over a switching period is illustrated in Fig. 9. The rectifier stage switches as presented in the previous section between two line-to-line voltages in order to produce sinusoidal input currents, which basically results in the splitting of the switching period in two unequal parts, during which we can assume the voltage delivered by the rectifier is constant. The inverter stage is producing a standard Space Vector Modulation switching pattern using each of the two unequal halves of the switching period as a given voltage source. Virtually, it compensates the difference between the two line-to-line voltages by operating in each switching period half with a different modulation index. The H-bridge is switching in an interleaved way in respect to the inverter stage, in order to allow the hybrid converter to produce all possible switching states, which makes possible to achieve the goal of correcting the rectified voltage, obtain decoupled control of the input and output voltages and to maintain the average capacitor voltage constant.

Because it is more convenient not to inject energy in the capacitor via an auxiliary supply, the control of the H-bridge should monitor the capacitor voltage which finally makes sure that the average energy flow in the capacitor is zero:

\[
\int V_{HB} \cdot I_{DC-INV} = 0 \quad \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cd 

Fig. 9. Switching states generation for a hybrid DPC

Fig. 10. Control signals for the three stages of the hybrid DPC

Fig. 11. Control diagram of the H-bridge inverter within the hybrid DPC
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Fig. 12. Operation of a 2-stage DPC with 10% voltage unbalance near overmodulation ($V_{out}/V_{in} = 0.86$) using passive compensation (left side); active compensation (right side) with $C_{clamp} = 52.5 \mu F$: (a) dc-link voltage; (b) low-pass filtered output voltages; (c) load currents; (d) input currents

The switching states of the three-stages of the hybrid converter which are using Space Vector Modulation in the rectifier and inversion stages is shown in Fig. 10 in the moment the average voltage generated by the H-bridge has to change sign. The control system that ensures the proper operation of the H-bridge inverter within the hybrid converter is shown in Fig. 11. The capacitor voltage is monitored by a PI controller in respect to its reference value and its output generates an offset which is added to the target average voltage seen by the inverter stage. This allows the hybrid converter to adapt to supply voltage changes. The average voltage delivered by the rectifier is calculated each switching period and subtracted from the target, which produces the reference voltage to be generated by the H-bridge inverter. By dividing this value to the actual H-bridge capacitor voltage, the duty-cycle of the nonzero voltage state of the H-bridge inverter is found, while its sign gives the combination of transistors that needs to be gated. A set of mono-stable flip-flops with settable delay perform the desired PWM generation.

6. Simulation Results

The operation of a DPC under unbalanced voltage supply has been previously investigated\(^{(15)(16)}\), but all the methods uses passive compensation which means that the available output voltage decreases as the unbalance increases. In order to prove the superiority of the proposed active compensation method, a simulation test is carried out where the DPC was required to supply the theoretical output voltage limit of 0.86 while the supply voltage has a 10% unbalance.

Fig. 13. Trajectory of (a)–(b) the input phase voltage and averaged output voltages vectors and (c)–(d) the grid input and output currents in the case of passive compensation (left side) and active compensation using the clamp circuit (right side) under 10% unbalance supply. $C_{clamp} = 52.5 \mu F$
6.1 Active Compensation Using the Clamp Capacitor

Fig. 12 shows that the output current and voltage are unbalanced when the input voltage is unbalanced at the maximum voltage transfer. It is also clear that the averaged output voltages were distorted when there is not enough dc link voltage to sustain the demand (Fig. 5(b)). With the use of the clamp voltage it was possible to maintain the output currents and voltages balanced and undistorted. It is required to have the reference input current vector angle aligned with the direct sequence of the input voltage vector to maintain the balanced input currents. This will create an extra distortion on the input side but will preserve the output converter performance. Fig. 13 shows the locus of the input voltage vector that is unbalanced (locus is an ellipse) and the locus of the averaged output voltage vector which in the case of no compensation, is clearly distorted due to insufficient voltage, while in case the active compensation is performed, it maintains circular shape. The effect on the output current is not so clear because the passive load attenuates the voltage distortion. As expected, the input current is more unbalanced in the case of active compensation.

6.2 Active Compensation Using the H-Bridge Inverter

A simulation model of the proposed hybrid converter topology has been built in Saber and the results of fully compensating the effects of unbalanced supply voltage on the output voltage delivered to the load are presented. Fig. 14(a) shows the unbalanced input phase voltages and
Fig. 14(b) reveals the waveforms of the input currents, which are slightly distorted (flat top) but well balanced. By utilizing the H-bridge it is possible to deliver sinusoidal and balanced output voltage near the maximum voltage transfer ratio. This can be seen in the shape of the load currents (Fig. 14(c)) and in the shape of the filtered output voltage (Fig. 14(d)). An RC filter with high cut-off frequency was used to extract the fundamental from the PWM output voltage in order to clearly show that the voltages are not only sinusoidal and balanced, but they are not decreased due to the fact that momentarily, due to unbalance, the input voltages cannot allow 0.86 voltage transfer ratio. The input and output voltage locus are shown in Fig. 14(e). It is clear that the input voltage is unbalanced. The hybrid converter operates near 0.86 voltage transfer ratio, which is denoted by the fact that the two waveforms are almost touching each other. Fig. 14(f) shows that both input and output currents are balanced, even though only the output current is sinusoidal. Balanced input currents in the circumstances of unbalanced supply voltage are obtained by circulating most of the power ripple drawn from the input side with the H-bridge capacitor.

In Fig. 15 are shown the intermediary link voltage seen at the rectifier side (top) and the intermediary link voltage and its average seen at the inverter side (bottom). The rectifier side voltage experience a minimum of 440 V of its average, while the inverter side stays almost constant at 500 V, which clearly prove the benefit of having the H-bridge inserted in the intermediary link. Fig. 16 offers closer look on the operation of the H-bridge inverter in order to determine what type of power devices and electrolytic capacitor needed. Fig. 16(a) reveals that the injected voltage reaches a peak of approx 90 V, which means that maintaining a 100 V reference in the capacitor voltage would avoid overmodulation. Fig. 16(b) shows that even though the size of the capacitor is small (1000 µF which actually stores the same energy as a 25 µF/630 V) and the voltage ripple is high (±10 V), it does not influence its behavior mainly because there is always a 90 degrees phase shift between the moment when the capacitor voltage reaches a minimum (which actually occurs when the injected voltage is zero) and the moment the injected reference voltage would reach a maximum. Fig. 16(c) shows the current that flows in the capacitor and its low-pass filtered waveform, which has its highest component (5.52 A_pk ≈ 3.9 A rms), at 100 Hz, which is revealed also by its spectrum presented in Fig. 16(d). As the second highest harmonic is at 300 Hz (3.21 A_pk ≈ 2.3 A rms), it means that the cumulative RMS capacitor current is approx. 4.6 A, which is very close to what a PEH169 series electrolytic capacitor (EVOX RIFA) can handle: 4.1 A@100 Hz for a 1000 µF/100 V or 5.0 A@100 Hz for a 1500 µF/100 V, which is far more that a high voltage electrolytic capacitor with equivalent energy stored (25 µF/630 V) can handle. Therefore, a film capacitor which is more expensive and bulkier would be needed for a back-to-back VSI with reduced dc-link capacitor operating under same level of unbalance.

7. Conclusions

A new method to perform active compensation of unbalanced supply voltage is proposed. It uses the clamp capacitor, which traditionally is used only for protection purpose and therefore, remains unused during normal operation in order to store some energy needed to correct the voltage deficit. It is proven through simulations that it can successfully compensate voltage unbalance as high as 10% without affecting the output voltage capability, which is the main concern when abnormal supply conditions occur. The price to be paid for improving the converter robustness against grid disturbances is a slightly oversized clamp capacitor, the need to introduce an extra IGBT in the clamp circuit and the degradation of input current quality due to uncontrolled capacitor charging.

In order to overcome this last disadvantage, a new hybrid power converter topology is proposed, which consists of connecting an H-bridge inverter into the intermediary circuit of an indirect matrix converter topology, between the rectifier and inverter stages. This allows for increased robustness against unbalanced supply voltage compared to the first method because of the fact that now the input currents are kept under control all the time, allowing for balanced input currents as proven by simulations. Furthermore, preliminary estimations show an improvement in the voltage transfer ratio from 0.866 to 0.909, which means that the voltage delivered to the output side falls within the normal voltage tolerance (±10%) of a motor which will allow this topology to directly compete the well established back-to-back voltage source converters.

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Appendix

1. Simulation parameters for topology shown in Figs. 12–13:
Input Filter: $C_{in} = 4.5\mu F$ star connected, $L_{in} = 1\text{ mH} (150\Omega \text{ parallel damping})$; Load: $R_L = 30\Omega$, $L_L = 5\text{ mH}$; $C_{Clamp} = 52.5\mu F$; $f_{sw} = 10\text{ kHz}$; $V_{in} = 397/397/457\text{ VRMS}/50\text{ Hz}$ ($V_{in-D} = 415\text{ VRMS}$); $V_{out} = 355\text{ VRMS}/40\text{ Hz}$; $[V_{out}/V_{in-D}]_{ref} = 0.86$.

2. Simulation parameters for topology shown in Figs. 14–16:
Input Filter: $C_{in} = 4.5\mu F$ star connected, $L_{in} = 1\text{ mH} (150\Omega \text{ parallel damping})$; Load: $R_L = 30\Omega$, $L_L = 5\text{ mH}$; $C_{HB} = 1000\mu F$; $V_{cap-ref} = 100\text{ V}$; $f_{sw} = 10\text{ kHz}$; $V_{in} = 397/397/457\text{ VRMS}/50\text{ Hz}$ ($V_{in-D} = 415\text{ VRMS}$); $V_{out} = 355\text{ VRMS}/40\text{ Hz}$; $[V_{out}/V_{in-D}]_{ref} = 0.86$.

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