Design and Implementation of an Impulse Commutated Solid-State Transfer Switch

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Keywords: voltage sag, solid-state transfer switch, thyristor, forced commutation, LC resonance

An impulse-commutated solid-state transfer switch (ICSTS) with a resonant commutation circuit is proposed. The thyristor-based solid-state transfer switch (STS) can utilize the dual power feeders to protect sensitive loads against voltage sags. Compared to gate-turn-off thyristors (GTOs), thyristors are favored for this application due to the lower conduction losses even though they can not self-commutate. For the conventional STS, the transfer process, which includes the detection of voltage sag and the thyristor commutation, may take up more than a quarter cycle. In this paper, the proposed ICSTS system can greatly reduce the transfer time and provide better protection against voltage sags.

For the conventional STS, the thyristor commutation is dependent on the voltage difference between the two feeders and the power factor of the load. The total transfer time of the conventional STS may exceed 10 ms in some situations. Such long transfer time could interrupt the operation of sensitive loads, and can not satisfy the requirement of industrial standards like the SEMI F47 standards. The proposed ICSTS greatly reduces the transfer time by using an impulse commutation circuit which consists of inductor L_r , capacitor C_r and a auxiliary semiconductor switch as shown in Fig. 1.

The impulse commutation circuits, which are placed across the thyristors on the primary feeder, are to expedite the commutation and to reduce the transfer time. Upon detection of voltage sags, the ICSTS controller will initiate the transfer process as follows:

1. Stop triggering the thyristors T1p (or T1n) on the primary feeder;
2. Start the LC resonance by triggering the auxiliary thyristors A11p (or A11n), and the current in the main thyristor will reduce and eventually reach cut-off;
3. Turn on the thyristors T2p (or T2n) on the alternate feeder to complete the load transfer.

Fig. 2 shows the details of the commutation process. As the sag is detected, the commutation is immediately initiated. The main thyristor is cut-off in approximately 25 μ s, which is much shorter

than the detection time. Therefore the thyristor commutation time of ICSTS can be neglected. The thyristor of the alternate feeder is triggered 128 μ s after the primary feeder thyristor is turned-off and the transfer process is completed.

The proposed ICSTS employs the impulse commutation circuit on the thyristors for fast turn-off, thus it can complete the transfer immediately upon the detection of voltage sags or swells. The laboratory test results validate that the proposed ICSTS can accomplish load transfer within 4–5 ms under most voltage sag and voltage swell situations. The conventional STS may require more than a quarter cycle to complete the transfer because of the dependence on the point-on-wave of sag occurrence and the power factor of the load, and it may require even more transfer time in case of voltage swells. The transfer time of ICSTS can meet the requirement of industry standards like SEMI F47. Test results validate the effectiveness of the ICSTS under voltage sag and voltage swell. Sensitive ASD load can also ride through voltage sags with the ICSTS. In general, the ICSTS provides better protection against voltage sags and swells than the conventional STS. A pre-charging scheme for the commutation circuit is also presented. Finally, the design procedures are presented to explain the sizing of the capacitor and the inductor of the impulse commutation circuit with respect to the characteristics of the main thyristor. The impulse commutation circuit can also utilize the surge current rating of the auxiliary thyristor for improved cost-effectiveness.

Fig. 1. Schematic diagram of the ICSTS system

Fig. 2. Detailed waveforms of the commutation. ($i_{th,pri}$, $i_{th,alt}$: X-axis: 40 μ s/div, Y-axis: 5 A/div; V_c : X-axis: 40 μ s/div, Y-axis: 40 V/div)

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In recent years, voltage sags have become a very important power quality issue. Voltage sags often interrupt manufacturing processes and result in significant losses. To improve the quality and reliability of electric power, more and more utility companies provide dual power feeders to high-tech manufacturers. The solid-state transfer switch (STS) based on thyristors can utilize the dual power feeders to protect sensitive loads against voltage sags. Conventional STS may require more than a quarter cycle to complete the transfer process depending on the operating condition of its loads. In this paper, an improved STS with resonant impulse commutation circuit is proposed. The proposed system can greatly reduce the transfer time and provide better protection against voltage sags. Laboratory test results are presented to validate the performance of the proposed STS system.

Keywords: voltage sag, solid-state transfer switch, thyristor, forced commutation, LC resonance

1. Introduction

Voltage sags of short durations often interrupt manufacturing processes and result in significant losses. In high-tech industry parks of Taiwan, manufactures may lose up to a million US dollars for each voltage sag event. To serve these high-tech manufacturers, utility companies have started providing dual power feeders to improve quality and reliability of electric power. The solid-state transfer switch (STS) based on thyristors, as illustrated in Fig. 1, can utilize the dual power feeder to protect sensitive loads against voltage sags⁽¹⁾. When a voltage sag occurs, the STS immediately transfer the loads from the faulted primary feeder to the alternate feeder to avoid interrupting the critical loads.

Thyristors have lower conduction losses compared to GTOs for medium-voltage applications⁽²⁾. However thyristors can not be turned-off by the their gate drivers. Therefore, for the conventional STS, the transfer process, which includes the detection of voltage sag and the thyristor commutation, may take up more than a quarter cycle.

In this paper, an impulse-commutated STS (ICSTS) with a

resonant commutation circuit is proposed. The proposed system can greatly reduce the transfer time and provide better protection against voltage sags. Forced commutation techniques have been used in high power thyristor-based converters with proven effectiveness. Solid state thyristor circuit breakers with forced commutation have also been proposed⁽²⁾⁽³⁾. This paper discusses the design of the proposed ICSTS and its control. Laboratory test results are presented to validate the performance of the proposed ICSTS system.

2. Voltage Sag Detection of the Proposed ICSTS System

Fig. 2 shows the simplified system diagram of the proposed ICSTS system. The control method for the ICSTS is based on the synchronous reference frame transformation (SRF)⁽⁴⁾.

$$\begin{bmatrix} v_{Pq}^e \\ v_{Pd}^e \end{bmatrix} = \begin{bmatrix} \cos(\omega_0 t) & -\sin(\omega_0 t) \\ \sin(\omega_0 t) & \cos(\omega_0 t) \end{bmatrix} \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & -\frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} v_{Pa} \\ v_{Pb} \\ v_{Pc} \end{bmatrix} \quad \dots\dots\dots (1)$$

A phase locked loop (PLL) is used to generate the grid frequency ω_0 (≈ 377 rad/sec). The positive sequence components of the primary feeder voltages v_{Pa} , v_{Pb} , v_{Pc} are transformed into the DC components of the synchronous frame voltages v_{Pq}^e , v_{Pd}^e . If the utility system operates in the normal condition, or if any symmetrical fault occurs, then v_{Pq}^e and v_{Pd}^e are DC quantities. If any unsymmetrical fault occurs, the resulting voltage sag is unbalanced and contains both the positive sequence and the negative sequence component, then the synchronous frame voltages v_{Pq}^e and v_{Pd}^e contain DC components and 120 Hz ripples. The proposed ICSTS controller uses the magnitude of the positive sequence component to determine if any voltage sag occurs. To implement this principle, the disturbance filters, which contains a notch at 120 Hz and a low-pass corner at 300 Hz as illustrated in Fig. 3, are employed to extract the DC components of v_{Pq}^e and v_{Pd}^e respectively⁽⁵⁾.

Fig. 1. Schematic diagram of a conventional STS system

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Fig. 2. Schematic diagram of the proposed ICSTS system

Fig. 3. Filtering characteristics of the disturbance filter

The DC components of v_{pq}^e and v_{pd}^e can be extracted by the disturbance filters to accomplish fast detection of voltage sag. The magnitude of the positive sequence component of the primary feeder voltage can be calculated as follows:

$$V_{pos} = \sqrt{(v_{pqF}^e)^2 + (v_{pdF}^e)^2} \dots \dots \dots (2)$$

The pre-fault values of v_{pqF}^e and v_{pdF}^e are latched and held in the controller to calculate the positive sequence voltage magnitude. A threshold level V_{th} is then determined by the stored pre-fault magnitude and a threshold factor k_{th} which usually lies between 0.8–0.9 depending on the sensitivity of critical loads. Once V_{pos} drops below V_{th} , then the controller can identify the voltage sag event and issues the transfer command. For the most part, the voltage sag detection scheme in the proposed ICSTS can identify voltage sags within 4 ms. Previous schemes proposed in ⁽⁴⁾⁽⁶⁾ usually require more than a quarter cycle.

The impulse commutation circuits, which are placed across the thyristors on the primary feeder as shown in Fig. 2, are to expedite the commutation and to reduce the transfer time. Upon detection of voltage sags, the ICSTS controller will initiate the transfer process as follows:

1. Stop triggering the thyristors T1p (or T1n) on the primary feeder;
2. Start the LC resonance by triggering the auxiliary

Fig. 4. Current flows during the resonant state

thyristors A11p (or A11n), and the current in the main thyristor will reduce and eventually reach cut-off;

3. Turn on the thyristors T2p (or T2n) on the alternate feeder to complete the load transfer.

3. Commutation and Load Transfer of the ICSTS

The detection time of the conventional STS depends on the point-on-wave of the sag occurrence ⁽⁶⁾. The voltage difference between the two feeders and the power factor of the load also affect the time needed for the commutation. Therefore, the conventional STS may require more than a quarter cycle to complete the transfer process.

The proposed ICSTS greatly reduce the transfer time by using an impulse commutation circuit which consists of L_r , C_r and auxiliary thyristors. Fig. 4, and 5 show the transfer process of the proposed ICSTS system. If the voltage sag is detected in the primary feeder and the load current flows through the thyristor T1p, the auxiliary switch A11p is turned on at $t = t_1$ to initiate the LC resonance and the current in T1p ($i_{th,pr}$ in Fig. 4 and 5) is suppressed. The load current is assumed constant during the resonant state ($t_1 \leq t \leq t_2$). At $t = t_2$, the current is smaller than the holding current of the thyristor, and T1p is turned off. The capacitor C_r continues to carry the load current and is discharged, and eventually the thyristor T2p becomes forward biased. At $t = t_3$, T2p is triggered and take over the load current, and the transfer process is completed.

Fig. 6 shows the details of the commutation process. The following assumptions are made to simplify the analysis:

1. All thyristors are ideal, no conduction voltage drop, no reverse recovery.

Fig. 5. A diagram of resonant state

Fig. 6. Commutation processes of the proposed ICSTS

2. Load current, primary feeder voltage, and the alternative feeder voltage remain constant during the commutation.
3. Line resistance is assumed to be zero.

Mode 0: $0 \leq t \leq t_1$

Since impulse commutation circuit must suppress the thyristor current at the any point of the its waveform, the following discussions assume that the line current is at its peak value when the voltage sag is detected and the commutation process is initiated as shown in Fig. 6(a).

$$V_C = V_{C0} \quad (3)$$

$$i_{th,pri} = I_{peak} \quad (4)$$

Mode 1: $t_1 \leq t \leq t_2$

In Fig. 6(b), the impulse commutation circuit is triggered upon the detection of the voltage sag to inject the resonant current i_r . The differential equation of resonant current is shown in (5).

$$\frac{d^2 i_r}{dt^2} + \frac{1}{L_r C_r} i_r = 0 \quad (5)$$

Solving the differential equation of i_r yields

$$i_r = i_{r,peak} \times \sin \omega_{r1}(t - t_1) \quad (6)$$

where

$$i_{r,peak} = V_{C0} \sqrt{\frac{C_r}{L_r}} \quad (7)$$

$$\omega_{r1} = \frac{1}{\sqrt{L_r C_r}} \quad (8)$$

To ensure that the current on the main thyristor can be cut off by the resonant current, the pre-charge voltage V_{C0} on capacitor has to satisfy the condition in (9).

$$V_{C0} \geq I_{peak} \sqrt{\frac{L_r}{C_r}} \quad (9)$$

The time needed to reach cut-off by the main thyristor is calculated in (10).

$$\Delta t_r = t_2 - t_1 \leq \frac{\pi}{2} \sqrt{L_r C_r} \quad (10)$$

Mode 2: $t_2 \leq t \leq t_3$

At the $t = t_2$, the resonant current reaches I_{peak} . The impulse commutation circuit carries this current until the alternate feeder is triggered as shown in Fig. 6(c).

$$i_r = I_{peak} = I_{Load} \quad (11)$$

Mode 3: $t_3 \leq t \leq t_4$

In Fig. 6(d), the thyristor on the alternate feeder is forward-biased when the thyristor on the primary feeder is turned off, therefore the load current is easily transferred to the alternate feeder as the alternative feeder thyristor is triggered. For simplicity, the primary feeder voltage V_{pri} and alternate feeder voltage V_{alt} are assumed constant during the commutation. This process is described in (12) by applying the Kirchoff's voltage law

$$V_{alt} - L_s \frac{d(I_{Load} - i_{pri})}{dt} = V_{pri} - (L_s + L_r) \frac{di_{pri}}{dt} + V_C \quad (12)$$

The above equation can be rewritten as

$$\frac{d^2 i_{pri}}{dt^2} + \frac{1}{(2L_s + L_r)C_r} i_{pri} = 0 \quad (13)$$

where the initial conditions are given as follows:

$$i_{pri}(t_3) = I_{peak} \quad (14)$$

and

$$\left. \frac{di_{pri}}{dt} \right|_{t=t_3} = \frac{C_r(V_{pri} - V_{alt}) - I_{peak}(t_3 - t_2)}{(2L_s + L_r)C_r} \quad (15)$$

i_{pri} can be obtained by solving (13):

$$i_{pri} = I_{peak} \cos \omega_{r2}(t - t_3) + \left(\frac{C_r(V_{pri} - V_{alt}) - I_{peak}(t_3 - t_2)}{\sqrt{(2L_s + L_r)C_r}} \right) \sin \omega_{r2}(t - t_3) \quad (16)$$

where

$$\omega_{r2} = \frac{1}{\sqrt{(2L_s + L_r)C_r}}$$

This mode ends when i_{pri} reduces down to zero at $t = t_4$, ie. $i_{pri}(t_4) = 0$. t_4 can be obtained by solving (16):

$$t_4 = t_3 + \sqrt{(2L_s + L_r)C_r} \left(\tan^{-1} \left(\frac{C_r(V_{pri} - V_{alt}) - I_{peak}(t_3 - t_2)}{I_{peak} \sqrt{(2L_s + L_r)C_r}} \right) - \frac{\pi}{2} \right) \quad (17)$$

4. Laboratory Test Results

A scaled-down prototype of the proposed ICSTS system is implemented in the laboratory, and the test bench is shown in Fig. 7. The test bench parameters are as follows:

- Source: 220 V, 60 Hz, and the transformer is rated at 5 kVA.
- Impulse Commutation circuit: $C_r = 4 \mu\text{F}$; $L_r = 16 \mu\text{H}$.
- Load: R-L load of 2.9 kVA, p.f. = 0.7; Inverter load of 220 V, 1.5 kW
- Controller: Threshold constant $k_{th} = 0.90$. The control method is implemented in a TMS320C6711 DSP, and the sampling frequency is 10 kHz.

4.1 Linear Load A single-phase grounded fault is introduced on the primary feeder. The fault results in a 57% of voltage sag in magnitude (line-to-neutral). The controller detects the voltage sag in 3.0 ms, the firing pulses to the main thyristors are immediately stopped, and the impulse commutation process initiated. As illustrated in Fig. 8 and Fig. 9, the primary feeder current on all three phases are cut off by the impulse commutation circuit. Fig. 10 shows the details of the commutation process. As the sag is detected, the commutation is immediately initiated. The main thyristor is cut-off in approximately 25 μs , which is much shorter than the detection time. Therefore the thyristor commutation time of ICSTS can be neglected. The LC resonance and the commutation is illustrated in Fig. 10. The thyristor of the alternate feeder is triggered 128 μs after the primary feeder thyristor is

Fig. 7. Laboratory test bench of the proposed ICSTS

Fig. 8. Line current on the primary feeder ($i_{a,pri}$, $i_{b,pri}$, $i_{c,pri}$: X-axis: 2 ms/div, Y-axis: 5 A/div; Sag command: X-axis: 2 ms/div, Y-axis: 5 V/div)

turned-off and the transfer process is completed. The current of both feeders of the proposed ICSTS is shown in Fig. 11.

Fig. 11 and Fig. 12 are to illustrate the fast commutation process of the proposed ICSTS compared to the conventional STS. In this test, the same voltage sag and the same detection method are used in the proposed ICSTS and the conventional STS to ensure the same voltage sag detection time for

Fig. 9. Current of the commutation circuits (i_{ra} , i_{rb} , i_{rc} : X-axis: 1 ms/div, Y-axis: 10 A/div; Sag command: X-axis: 1 ms/div, Y-axis: 5 V/div)

Fig. 10. Detailed waveforms of the commutation ($i_{th,pri}$, i_r , $i_{th,alt}$: X-axis: 40 μs /div, Y-axis: 5 A/div; V_c : X-axis: 40 μs /div, Y-axis: 40 V/div)

Fig. 11. The load current of the proposed ICSTS (Sag command, Transfer command: X-axis: 4 ms/div, Y-axis: 5 V/div; i_{pri} , i_{alt} : X-axis: 4 ms/div, Y-axis: 10 A/div)

Fig. 12. The load current of the conventional STS (*Sag* command, *Transfer* command: X-axis: 4 ms/div, Y-axis: 5 V/div; i_{pri} , i_{alt} : X-axis: 4 ms/div, Y-axis: 10 A/div)

comparison. In both cases, the transfer commands are issued 3.0 ms after the fault occurs. For the conventional STS, the alternate feeder thyristor can not be triggered until the primary feeder thyristor is cut-off. As a result, the conventional STS completes the transfer 2.4 ms after the transfer command is issued as shown in Fig. 12. In comparison, the ICSTS completes the transfer immediately right after the transfer command is issued as shown in Fig. 11. The load voltages of both STS systems are in Fig. 13, 14 respectively. When the transfer command is issued, the ICSTS transfer the load to the alternate feeder and restore the load voltage instantly to the normal level (310 V for $V_{ab,load}$ and -120 V for $V_{bc,load}$). On the other hand, the conventional STS still remains under the sag condition (235 V for $V_{ab,load}$ and -40 V for $V_{bc,load}$) when the transfer command is issued. The conventional STS completes the transfer almost 2.4 ms after the command is issued. The proposed ICSTS can transfer the load immediately upon detection of voltage sags, thus provide better protection than the conventional STS.

4.2 Inverter Load The adjustable speed drive (ASD) is widely used by industries. The under voltage protection of ASDs is often triggered when the voltage sags occur, then leads to unexpected shutdown. In this test, a commercial ASD is used as the critical load to verify the performance of the proposed ICSTS. The controller takes 3.2 ms to detect the voltage sag when the single-phase grounded fault occurs. Fig. 15 shows that the diode rectifier current is interrupted momentarily by the sag and then resumes immediately as being transferred to the alternate feeder. After the commutation, the capacitor bank in the inverter DC link is recharged and causes the input current surge. Also, Fig. 16 shows the load voltages reduce due to the sag and recover immediately after the transfer. The ASD under test operates normally without being interrupted by the voltage sag.

4.3 Voltage Swell The voltage swell may occur in the utility grid due to switching off a large load or energizing a large capacitor bank⁽⁷⁾. The voltage swell may trigger the overvoltage protection in the sensitive load. The conventional STS may need more than half cycle to transfer the load to the alternate feeder because the primary feeder has higher voltage potential than alternate feeder, the thyristors on alternate feeder can not be gated on until the primary feeder

Fig. 13. The load voltages of the proposed ICSTS ($V_{ab,load}$, $V_{bc,load}$, $V_{ca,load}$: X-axis: 10 ms/div, Y-axis: 400 V/div; *Transfer* command: X-axis: 10 ms/div, Y-axis: 5 V/div)

Fig. 14. The load voltages of the conventional STS ($V_{ab,load}$, $V_{bc,load}$, $V_{ca,load}$: X-axis: 10 ms/div, Y-axis: 400 V/div; *Transfer* command: X-axis: 10 ms/div, Y-axis: 5 V/div)

Fig. 15. The line current of the proposed ICSTS (i_{alt} , i_{pri} , i_{load} : X-axis: 10 ms/div, Y-axis: 10 A/div; *Sag* command: X-axis: 10 ms/div, Y-axis: 5 V/div)

thyristors naturally commutates.

The ICSTS is tested under the voltage swell. In this experiment, the threshold constant is set at 1.2 p.u. ($k_{th} = 1.2$) for the detection of voltage swells. Under the normal operation, the current goes through the primary feeder to the

Fig. 16. The load voltages of the proposed ICSTS ($V_{ab,load}$, $V_{bc,load}$, $V_{ca,load}$: X-axis: 10 ms/div, Y-axis: 400 V/div; Sag command: X-axis: 10 ms/div, Y-axis: 5 V/div)

Fig. 17. The voltage swell in primary feeder ($V_{ab,pri}$, $V_{bc,pri}$, $V_{ca,pri}$: X-axis: 20 ms/div, Y-axis: 400 V/div; Swell command: X-axis: 20 ms/div, Y-axis: 5 V/div)

Fig. 18. The transfer process of the proposed ICSTS (V_{pri} , V_{alt} : X-axis: 4 ms/div, Y-axis: 400 V/div; i_{pri} , i_{alt} : X-axis: 4 ms/div, Y-axis: 5 A/div)

load, and the line voltage is kept at 220 V. When the voltage swell occurs, the line voltage of primary feeder rises to 330 V instantly as shown in Fig. 17. Fig. 18 shows that the ICSTS completes the transfer in approximately 4.4 ms, Fig. 19 shows the transfer of the conventional STS with the same detection method under the same voltage swell. The conventional STS

Fig. 19. The transfer process of the conventional STS (V_{pri} , V_{alt} : X-axis: 4 ms/div, Y-axis: 400 V/div; i_{pri} , i_{alt} : X-axis: 4 ms/div, Y-axis: 5 A/div)

Fig. 20. (a) Pre-charge of C_m ; (b) T1p is triggered when C_m is charged to the desired level; (c) The critical load is placed back to the primary feeder after the pre-charge

needs 9.6 ms to complete the transfer, 5.2 ms more than the proposed ICSTS. The reason is that the primary feeder has higher voltage potential than the alternate feeder, the thyristors of the alternate feeder are reverse-biased and can not be triggered until the primary feeder thyristor commutate naturally.

4.4 Capacitor Pre-charge The resonant capacitors (C_{rn} and C_{rp}) must be sufficiently charged for the forced commutation. The pre-charge process for the laboratory test-bench is illustrated in Fig. 20. During the pre-charge, the main thyristors T1p and T1n are not triggered. The auxiliary thyristor A12n is gated on to charge C_{rn} during the positive half cycle of the charging current, and the main thyristor T1p is triggered when the voltage of C_{rn} reaches the desired level as shown in Fig. 20(b). The capacitor C_{rp} can be charged similarly in the negative half cycle of the charging current. Fig. 21 shows voltages of C_{rp} and C_{rn} are charged to approximately the peak value of the line-to-neutral voltage. The critical load is powered by the alternative feeder to avoid any interruption as capacitors are being charged. After the pre-charge is completed, the charging resistor is taken off-line (turn-off S2), and the critical load is transferred back to the primary feeder smoothly by naturally commutate the

Fig. 21. Pre-charge of the capacitor voltage (Line current: X-axis: 4 ms/div, Y-axis: 10 A/div; Line-to-neutral voltage, V_{cn} , V_{cp} : X-axis: 4 ms/div, Y-axis: 100 V/div)

alternate feeder thyristors at an appropriate moment. Now the critical load is fed by the primary feeder as in Fig. 20(c) and the ICSTS is ready if transfer command is issued upon detection of any voltage sags. This scheme offers the advantages of short charging time (typically within one cycle) and a controllable pre-charge voltage. The capacitor voltage can be maintained by using a small power supply. Other charging scheme using passive components (such as diodes and varistors) have also been proposed⁽⁸⁾.

5. Discussions

In this section, design issues of the ICSTS are discussed in detail. Fig. 22 shows the turn-off waveforms of the thyristor. For a successful commutation, sufficient initial charge in the capacitor C_r is needed to commutate the maximum load current, to overcome the thyristor reverse recovery and to satisfy the turn-off time requirement of the thyristor. To prevent excessive voltage spikes on the load voltage during the commutation, the pre-charge voltage of C_r must be limited. The following procedures show how the impulse commutation circuit can be designed under a pre-determined initial voltage V_{C0} .

Step 1: The resonant inductor L_r is to limit the rise time of the commutation current to avoid damaging the auxiliary thyristor in the commutation circuit. The restriction of L_r is given in (18):

$$L_r \geq V_{C0} \cdot \left(\frac{di_r}{dt} \Big|_{critical} \right)^{-1} \quad (18)$$

where $di_r/dt|_{critical}$ is the critical rate of rise of the auxiliary thyristor current.

Step 2: To commutate successfully, the main thyristor must be reversed-biased throughout the reverse-recovery period (t_{rr}) and the turn-off time period (t_q). The required voltage ($\Delta V_{rr} + \Delta V_{hold}$) illustrated in Fig. 22 can be estimated as given in (19) and (20) across the thyristor to guarantee cutting-off the thyristor current during the turn-off interval.

$$\Delta V_{rr} = \frac{I_{peak}}{C_r} t_{rr} + \frac{Q_{rr}}{C_r} \quad (19)$$

$$\Delta V_{hold} = \frac{I_{peak}}{C_r} (t_q - t_{rr}) \quad (20)$$

Fig. 22. Turn-off transient of thyristor

where Q_{rr} is the stored charge. The reverse recovery time t_{rr} is can be expressed as:

$$t_{rr} = \sqrt{\frac{2 \cdot Q_{rr}(1+S)}{\frac{di_r}{dt}}} \quad (21)$$

where S is the snappiness factor of the main thyristor.

$$S = \frac{t_f}{t_s} \quad (22)$$

Solving the differential equation of i_r (Equation (5)) yield

$$i_r = V_{C0} \sqrt{\frac{C_r}{L_r}} \times \sin(\omega_r t), \quad \omega_r = \frac{1}{\sqrt{L_r C_r}} \quad (23)$$

Assume that the load current is at its peak value I_{peak} when the transfer command is issued. The resonant current i_r rises and then reaches the value of I_{peak} . The main thyristor current reaches zero while the commutation current i_r reaches I_{peak} at $t = t_r$.

$$i_r(t_r) = I_{peak} = V_{C0} \sqrt{\frac{C_r}{L_r}} \times \sin(\omega_r t_r) \quad (24)$$

The resonant time t_r can be expressed as

$$t_r = \frac{1}{\omega_r} \sin^{-1} \left(\frac{I_{peak}}{V_{C0}} \sqrt{\frac{L_r}{C_r}} \right) \quad (25)$$

The capacitor voltage can be expressed as

$$v_c = \frac{1}{C_r} \int_0^t -i_r dt + V_{C0} = V_{C0} \cos(\omega_r t) \quad 0 \leq t \leq t_r \quad (26)$$

At $t = t_r$ the main thyristor current is down to zero, the capacitor voltage v_c must be at least ($\Delta V_{rr} + \Delta V_{hold}$) to avoid any re-triggering during the reverse-recovery and the turn-off time.

$$v_c(t_r) = V_{C0} \cos(\omega_r t_r) \geq \Delta V_{rr} + \Delta V_{hold} \quad (27)$$

By substituting t_r of (25) into (27) yields

$$V_{C0} \geq \frac{\Delta V_{rr} + \Delta V_{hold}}{\cos(\omega_r t_r)} = \frac{\frac{Q_{rr}}{C_r} + \frac{I_{peak} t_q}{C_r}}{\cos\left(\sin^{-1}\left(\frac{I_{peak}}{V_{C0}} \sqrt{\frac{L_r}{C_r}}\right)\right)} \dots \dots \dots (28)$$

where

$$\cos\left(\sin^{-1}\left(\frac{I_{peak}}{V_{C0}} \sqrt{\frac{L_r}{C_r}}\right)\right) = \sqrt{1 - \left(\frac{I_{peak}}{V_{C0}} \sqrt{\frac{L_r}{C_r}}\right)^2}$$

Equation (28) can be rewritten as

$$\frac{V_{C0}}{I_{peak}} \sqrt{\frac{C_r}{L_r}} \geq \sqrt{\frac{1}{L_r C_r} \left(\frac{Q_{rr}}{I_{peak}} + t_q\right)^2} + 1 \dots \dots \dots (29)$$

Therefore, for a pre-determined V_{C0} , C_r must satisfy

$$C_r \geq \frac{L_r}{2} \left(\frac{I_{peak}}{V_{C0}}\right)^2 \left(1 + \sqrt{1 + \left(\frac{2}{L_r} \left(\frac{Q_{rr}}{I_{peak}} + t_q\right) \frac{V_{C0}}{I_{peak}}\right)^2}\right) \dots \dots \dots (30)$$

Equation (30) gives the minimum requirement of the capacitor size under a pre-determined initial voltage V_{C0} . If the turn-off time t_q of the main thyristor is long, a larger capacitor will be required for a successful commutation.

Step 3: Since auxiliary thyristor conducts current only when the forced-commutation is in progress, its surge capability can be utilized to complete the commutation process. From (31) the expression of the maximum resonant current $i_{r,peak}$ which the auxiliary thyristor must withstand is given as

$$i_{r,peak} = I_{peak} + \Delta i_{rr} \dots \dots \dots (31)$$

where Δi_{rr} is the reverse-recovery current of the main thyristor given as in (32):

$$\Delta i_{rr} = \frac{2Q_{rr}}{t_{rr}} = \sqrt{\frac{2 \cdot Q_{rr} \cdot \frac{di_r}{dt}}{(1+S)}} \dots \dots \dots (32)$$

A design example is given to validate the design process. Critical loads of 300 kVA (pf = 0.7 lagging) installed on a 480 V bus are to be protected by the proposed ICSTS. A commercially available thyristor (SKT-1000/12E, 1000 A, 1200 V) is used as the main thyristors of ICSTS, and a smaller thyristor (SKT-80/12E, 80 A, 1200 V, surge current of 1500 A at 130°C) is chosen as the auxiliary thyristors. By the pre-charging scheme, the initial voltage of 383 V, which is close to the peak value 392 V of the line-to-neutral voltage, is stored in the resonant capacitors. For the auxiliary thyristor SKT-80/12E, di/dt must be limited below 50 A/us, thus the inductor $L_r = 18 \mu\text{H}$ can be obtained from (18). The reverse recovery charge Q_{rr} of the main thyristor SKT-1000/12E is approximately 2.3 mC at 600 A under di/dt of 50 A/us, and the maximum turn-off time t_q is approximately 250 us. Therefore, by (30), the minimum capacitance of 420 μF is required with the pre-charge voltage of 383 V. Fig. 23 shows the pre-charge voltage versus the size of the capacitor under different turn-off time t_q . Longer turn-off time of the main

Fig. 23. Pre-charge voltage (V_{C0}) v.s. Size of capacitor (C_r)

thyristor requires more stored charge as illustrated. Proper combinations of pre-charge voltage and capacitor can be selected along the curve to satisfy the requirement of successful commutation.

The auxiliary thyristor must withstand the maximum resonant current $i_{r,peak}$ during the commutation process. Since the maximum resonant current $i_{r,peak}$ is affected by the snap-piness factor S of the main thyristor as in (32), the worst case condition of $S \approx 0$ and the resulting maximum Δi_{rr} is assumed. From (32), the maximum recovery current Δi_{rr} of 313 A can be calculated, and the maximum current through the impulse commutation circuit ($I_{peak} + \Delta i_{rr}$) is approximately 913 A, which is within the surge current constraint of the auxiliary thyristor.

Based on the specifications of the main and the auxiliary thyristors and the rating of the loads, the design procedures provide an effective estimation of the required inductor and the capacitor based on a given pre-charge voltage.

6. Conclusions

An impulse commutated solid-state transfer switch (ICSTS) is proposed in this paper. Together with the SRF based control method, the proposed ICSTS can accomplish load transfer within 4–5 ms under most voltage sag and voltage swell situations by tuning the bandwidth of the disturbance filter and the threshold factor k_{th} of the controller. The conventional STS may require more than a quarter cycle to complete the transfer because of the dependence on the point-on-wave of sag occurrence and the power factor of the load, and it may require even more transfer time in case of voltage swells as shown in the test results. The proposed ICSTS employs the impulse commutation circuit on the thyristors for fast turn-off, thus it can complete the transfer immediately upon the detection of voltage sags or swells. The transfer time of ICSTS can meet the requirement of industry standards like SEMI F47⁽⁹⁾. Test results validate the effectiveness of the ICSTS under voltage sag and voltage swell. Sensitive ASD load can also ride through voltage sags with the ICSTS. In general, the ICSTS provides better protection against voltage sags and swells than the conventional STS. A pre-charging scheme for the commutation circuit is also presented. Finally, the design procedures are presented to explain the sizing of the capacitor and the inductor of the

impulse commutation circuit with respect to the characteristics of the main thyristor.

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