High-Speed Analysis of Bus Bar Inductance for a Laminated Structure

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In power converter circuits, the stray inductance of a bus bar between a DC capacitor and power devices may affect overvoltage and influence the switching losses under high-speed switching operation. Therefore, it is necessary to design the wiring structure by considering the stray inductance of the bus bar.

The authors have proposed an inductance map, which depicts the relationship between the wiring structure and the stray inductance. The inductance map is useful for an initial design of the circuit structure. This paper proposes two high-speed analysis methods for drawing the inductance map of the laminated bus bar structure. These methods are based on the symmetric bus bar structure and searching method of specific inductance. As a result, the computation speed of the proposed method is more than ten times higher than that of the conventional method. In addition, the experimental results rated at 500 V and 70 A for a buck chopper circuit using SiC-MOSFET and SiC-SBD confirm the usefulness of the design procedure.

Keywords: bus bar, inductance map, laminated structure, stray inductance

1. Introduction

Recently, silicon carbide (SiC) power devices have been developed to achieve high-switching-frequency, high- di/dt , and high- dv/dt switching operation. It is important to analyze the DC-side stray inductance between the DC capacitor and power devices because this may affect the switching losses and lead to the occurrence of overvoltage in power devices. Therefore, a number of papers have presented these effects using calculations, experiments, and circuit simulations^{(1)–(8)}. Thus, it is necessary to design the wiring structure of the circuit with consideration of the stray inductance. If the stray inductance can be designed, then the overvoltage and switching losses can be analyzed precisely.

A number of researches have investigated the stray inductance of the bus bar for a specific structure using 3D-FEA (Three-Dimensional Finite Element Analysis), and low-inductance structures have been proposed⁽⁵⁾. A partial inductance calculation method has been proposed as another method to simply calculate the stray inductance^{(9)–(12)}. In order to design the DC-side wiring structure of power converter circuits by consideration of the stray inductance, it is essential to clarify the relationship between the wiring structure and stray inductance. However, the design procedure for the wiring structure for power converter circuits has not yet been discussed.

The authors have proposed an inductance map which is the relationship between the wiring structure and stray inductance. The inductance map is useful for an initial design of the circuit structure. The inductance map is drawn using a partial inductance calculation method without using

3D-FEA. In addition, the design procedure for the wiring structure with consideration of the stray inductance of the bus bar is shown using the inductance map⁽¹⁾. This paper proposes two high speed analysis methods; quarter analysis and specific inductance searching for a laminated structure. This paper presents three types of DC-side bus bars for a buck chopper circuit, and overvoltage of the MOSFET will be discussed under high-speed switching operation. Moreover, the experimental results obtained using SiC-MOSFET and SiC-SBD (Schottky Barrier Diode) confirm the validity of the design procedure.

2. Partial Inductance Calculation Method

A partial inductance calculation method for bus bars has been proposed^{(9)–(12)}. Fig. 1 shows a simplified model for a laminated bus bar structure, and Fig. 2 shows the analytical model for partial inductance calculation method. The bus bar structures and the partition model are used for the following analysis. Bus bars A and B have cross-sections $t \times w$ and line length ℓ are arranged in parallel. They are divided into an n -piece conductor having a square cross section, and the conductors of bus bars A and B are denoted 1, 2, $\dots$, n , and 1', 2', $\dots$, n' , respectively. The division numbers can be set to the following equation

$$n = \frac{w}{t} \dots \dots \dots (1)$$

As a result, the division number defines the structure of the bus-bar. The relationship between the calculation error and the division numbers are discussed in detail in Ref(1). The following conditions are assumed in the calculation.

- In the case of calculating the self-inductance, the current in each conductor is regarded to be distributed uniformly on the circular cross-section.

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Fig. 1. Simplified laminated bus bar structure

Fig. 2. Analytical bus bar model for the partial inductance calculation method

Fig. 3. Equivalent circuit for the two bus bars

- In the case of calculating the mutual inductance, the current in each conductor flows through the center of the conductor in the lengthwise direction.
- No resistance component exists in the conductors, because of simply calculation.

Fig. 3 shows an equivalent circuit including the self- and mutual-inductances of the two bus bars. The voltages and currents are given by:

$$\begin{bmatrix} V_A \\ V_B \end{bmatrix} = j\omega \begin{bmatrix} L_A & M_{A,B} \\ M_{B,A} & L_B \end{bmatrix} \cdot \begin{bmatrix} I_A \\ I_B \end{bmatrix} \dots\dots\dots (2)$$

where, ω is the angular frequency of V_A , V_B , I_A , I_B . L_A and L_B are the self-inductance matrices of the bus bars and $M_{A,B}$ and $M_{B,A}$ are the mutual inductance matrices between the bus bars. The inductance matrix L_B is equal to L_A when the bus bars have the same shape and number of partitions. In addition, V_A , V_B , I_A , and I_B are n -row, one-column vectors that indicate the voltages and currents of n individual conductors.

Fig. 4. Circular partition method

$$L_A = L_B = \begin{bmatrix} L_1 & M_{1,2} & \dots & M_{1,n} \\ M_{2,1} & L_2 & \dots & M_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ M_{n,1} & M_{n,2} & \dots & L_n \end{bmatrix} \dots\dots\dots (3)$$

$$M_{A,B} = \begin{bmatrix} M_{1,1'} & M_{1,2'} & \dots & M_{1,n'} \\ M_{2,1'} & M_{2,2'} & \dots & M_{2,n'} \\ \vdots & \vdots & \ddots & \vdots \\ M_{n,1'} & M_{n,2'} & \dots & M_{n,n'} \end{bmatrix} \dots\dots\dots (4)$$

$$M_{B,A} = \begin{bmatrix} M_{1',1} & M_{1',2} & \dots & M_{1',n} \\ M_{2',1} & M_{2',2} & \dots & M_{2',n} \\ \vdots & \vdots & \ddots & \vdots \\ M_{n',1} & M_{n',2} & \dots & M_{n',n} \end{bmatrix} \dots\dots\dots (5)$$

$$V_A = \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_n \end{bmatrix}, \quad V_B = \begin{bmatrix} V_{1'} \\ V_{2'} \\ \vdots \\ V_{n'} \end{bmatrix}, \quad I_A = \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_n \end{bmatrix}, \quad I_B = \begin{bmatrix} I_{1'} \\ I_{2'} \\ \vdots \\ I_{n'} \end{bmatrix} \dots\dots\dots (6)$$

The self-inductance L_i ($i = 1 \sim n$) of the conductors in Eq. (3) can be calculated based on the cross-section and length of the conductors. The self-inductance of a conductor with a circular cross-section L_c as shown in Fig. 4, can also be calculated. Therefore, this method does not use any approximation for ℓ , but uses an approximation based on the cross-sectional area. In this case, L_c can be calculated with the following equation,

$$L_c = \frac{\mu_0 \ell}{8\pi} + \frac{\mu_0}{2\pi} \left(\ell \ln \frac{\sqrt{r^2 + \ell^2} + \ell}{r} - \sqrt{r^2 + \ell^2} + r \right) \dots\dots\dots (7)$$

where r is the radius of the circular cross-section of the conductors, and is set to $t/2$.

In addition, the mutual-inductance between two conductors $M_{i,j}$ ($i = 1 \sim n$, $j = 1' \sim n'$) in Eqs. (3) and (4) can be calculated without considering the cross section⁽⁹⁾. Therefore, $M_{i,j}$ is given by

$$M_{ij} = \frac{\mu_0}{2\pi} \left(\ell \ln \frac{\sqrt{(d+2r)^2 + \ell^2} + \ell}{(d+2r)} - \sqrt{(d+2r)^2 + \ell^2} + (d+2r) \right) \dots\dots\dots (8)$$

All of the conductors are connected in parallel to each bus bar so that the voltage across each conductor is the same ($V_A = V_1 = V_2 = \dots = V_n$, $V_B = V_{1'} = V_{2'} = \dots = V_{n'}$).

In addition, the total current in each bus bar is the sum of the currents of these conductors ($I_A = I_1 + I_2 + \dots + I_n$, $I_B = I'_1 + I'_2 + \dots + I'_n$). The following equation is given by the inverse of the matrix in Eq. (2) with these conditions, where $b_{i,j}$ is the element of the calculated inverse matrix in Eq. (2).

$$\begin{bmatrix} I_A \\ I_B \end{bmatrix} = \frac{1}{j\omega} \begin{bmatrix} \sum_{i=1}^n \sum_{j=1}^n b_{i,j} & \sum_{i=1}^n \sum_{j=1'}^{n'} b_{i,j} \\ \sum_{i=1'}^{n'} \sum_{j=1}^n b_{i,j} & \sum_{i=1'}^{n'} \sum_{j=1'}^{n'} b_{i,j} \end{bmatrix} \cdot \begin{bmatrix} V_A \\ V_B \end{bmatrix} \dots\dots\dots (9)$$

Moreover, the following equation is given by the inverse of the matrix in Eq. (9) to solve for V_A and V_B .

$$\begin{bmatrix} V_A \\ V_B \end{bmatrix} = j\omega \begin{bmatrix} L_A & M_{A,B} \\ M_{B,A} & L_B \end{bmatrix} \cdot \begin{bmatrix} I_A \\ I_B \end{bmatrix} \dots\dots\dots (10)$$

where L_A and L_B are the self-inductances of bus bars A and B, and $M_{A,B}$ and $M_{B,A}$ are the mutual inductances between bus bars A and B. In this case, the total inductance of the two bus bars can be calculated as follows.

$$L_{\text{cal}} = 2(L_A - M_{A,B}) \dots\dots\dots (11)$$

3. High-Speed Analysis Procedure

3.1 Symmetric Bus Bar Structure The laminated structure as shown in Fig. 2, the mutual inductances in each conductor are given by

$$M_{i,j} = M_{j,i} = M_{n-i+1,n-j+1} = M_{n-j+1,n-i+1} \dots\dots\dots (12)$$

Because the structure of the bus bar and current directions in each conductor are symmetric. In this case, each element of the inverse matrix in Eq. (9) is also given by as following.

$$b_{i,j} = b_{j,i} = b_{n-i+1,n-j+1} = b_{n-j+1,n-i+1} \dots\dots\dots (13)$$

Therefore, the matrix in Eq. (9) can be represented by

$$\begin{bmatrix} \sum_{i=1}^n \sum_{j=1}^n b_{i,j} & \sum_{i=1}^n \sum_{j=1'}^{n'} b_{i,j} \\ \sum_{i=1'}^{n'} \sum_{j=1}^n b_{i,j} & \sum_{i=1'}^{n'} \sum_{j=1'}^{n'} b_{i,j} \end{bmatrix} = \begin{bmatrix} 2 \sum_{i=1}^n \sum_{j=1}^{n/2} b_{i,j} & 2 \sum_{i=1}^n \sum_{j=1}^{n'/2} b_{i,j} \\ 2 \sum_{i=1}^{n'} \sum_{j=1}^{n/2} b_{i,j} & 2 \sum_{i=1}^{n'} \sum_{j=1}^{n'/2} b_{i,j} \end{bmatrix} \dots\dots\dots (14)$$

As a result, the analysis region of the matrix can be modified within $1 \leq i \leq n'$ and $1 \leq j \leq \frac{n}{2}$, therefore the computational complexity of this analysis method using Eq. (14) is a quarter less than that of the conventional method. In the following sections, this analysis is defined as a quarter analysis.

3.2 Comparison of Computation Times The computation time for the four calculation methods are discussed, where an Intel(R) Core i5 3.3 GHz, with 8 GB memory is used for the analysis methods. Fig. 5 shows the computation time for each analysis method, where the horizontal axis is division numbers n of the conductors and the vertical axis is the computation time.

The red line shows a conventional method⁽¹⁾ using Eq. (9) based on conjugate gradient (CG) method, and the blue line means the analysis results of the quarter analysis method using Eq. (14) based on the CG method. The computation time of the quarter analysis of the blue line is quarter as fast as

Fig. 5. Relationship between computation time and division number on a bus bar structure

Fig. 6. Search method for a specific value

that of the conventional analysis of the red line. Moreover, the preconditioning conjugate gradient (PCG) method is applied to the quarter analysis as indicated by the black line, because the PCG method is suitable for the numerical solution of systems of linear equations with the symmetric matrices. The PCG method is applicable to the conventional analysis method as shown in green line.

For example, when the division number n is set to 100, the computation time of the quarter analysis with the PCG method is 10 times as fast as that of the conventional analysis with CG method. Moreover, it can be confirmed that the advantage of the PCG method with increasing the division number.

3.3 Searching Method for a Specific Inductance

Long computation times are required for analysis procedure described in the previous section, because many analytical points are needed. In order to reduce the computation time, this section proposes a searching method for a specific inductance based on the inductance map. As a result, this method can significantly reduce the computation time.

The following procedure is the algorithm for the searching method, and Fig. 6 shows how to search for the specific inductance. The blue line assumes true values L_O , and the red squares (a) ~ (i) are the search points L_C . The initial analytical point is set to point (a), and Δl is changed to find the specific inductance at first.

- (1) Initial point (a): It is difficult to find the specific inductance in the analytical region. The initial point of the analysis is set to the following point; $\ell=0$, and d is set to the maximum value at the upper left in the analytical region.
- (2) In the case of $L_C > L_O$ at points (c), (d), and (g): ℓ is fixed at a constant value, and d is decreased by Δd . Hence, L_C can be changed by a small amount.

- (3) In the case of $L_C < L_O$ at points (a), (b), (e), (f), and (h): d is fixed at a constant value, and ℓ is increased by $\Delta\ell$. Hence, L_C can be changed by a large amount.

4. Relationship between the Wiring Structure and the Stray Inductance of the Bus Bars

4.1 Inductance Map Fig. 7 shows the total inductance map of the laminated structure. The total inductance of the laminated bus bar depends on both ℓ and d . The relationship between the wiring structure and stray inductance of the bus bar is clarified based on these inductance maps. There are 40,000 analytical models in these maps, and drawing these maps requires 1560 seconds. In this case, the distance and length step of this analysis Δd and $\Delta\ell$ are set to 0.1 mm and 1 mm, respectively. The purpose of drawing the inductance map is to know the relationship between the structure and inductance, so it is sufficient the resolution less than 1% of the distance d and the length ℓ .

4.2 Specific Inductance Map Fig. 8 shows the specific inductance map for the laminated bus bar of 40 nH, where t and w are set to 0.5 and 50 mm, respectively. The inductance is the sum of the bus bar inductance L_{total} and the wiring inductance of 24 nH around the power devices. The red line shows only the equivalent inductance line of 40 nH. The $\Delta\ell$ is set to 1 mm, and Δd is set to 0.1 mm.

4.3 Comparison of Computation Times for the Inductance Map Table 1 summarizes the comparison for the total computation time of the inductance maps, where the division numbers of the conductors n are set to 100. The conventional inductance map, as shown in Fig. 7, requires 1560 seconds, but the specific inductance map, as shown in

Fig. 7. Inductance map for the laminated bus bar ($t=0.5$ mm, $w=50$ mm)

Fig. 8. Specific inductance map for the laminated bus bar of 40 nH ($t=0.5$ mm, $w=50$ mm)

Fig. 8, requires only 38 seconds. The analysis of both inductance maps are applied to the quarter analysis with the PCG method. The analysis points of the conventional inductance map are 8 times higher than the specific inductance map. From these results, the specific inductance map is suitable for the initial design of the bus bar structure.

5. Design of DC-side Bus Bars and Experimental Verification

5.1 Bus Bar Structures Three types of DC-side bus bars (bus bar I, II, and III) are designed at the conditions denoted by the $\circ$ symbols in Fig. 8; therefore, the designed inductance L_{cal} of bus bars I~III are set to the same inductance of 40 nH. The length ℓ of the bus bar III is twice as long as that of the bus bar I, and the distance d of the bus bar I is 3.8 times as long as that of bus bar III.

Table 3 shows the bus bar parameters used in the experiments. In this case, the cross section $t \times w$ of the bus bar was set to 25 mm², and the current rating of the bus bar was set to 100 A.

5.2 Experimental Setup Fig. 9 shows the buck chopper circuit, and Table 2 shows the circuit parameters. The output side of the chopper circuit is only connected to the air-core inductor L , because double-pulse experiments were applied. The SiC-MOSFET and SiC-SBD rated at 1,200 V were used in this experimental circuit, and the DC voltage was set to 500 V. The drain current i_D at the turn-off is set to 70 A which is the rated pulse current. This circuit does not contain a snubber circuit around the power devices, and no external gate resistance was connected to the MOSFET because high-speed switching operation was assumed. However, the SiC-MOSFET is connected to a 5 Ω gate resistance inside the module.

Figs. 10 and 11 show the experimental setup and the PCB (Printed Circuit Board) layout of the chopper circuit,

Table 1. Total computation time of the inductance maps

	Fig. 7	Fig. 8
Computation Time	1,560 seconds	38 seconds
Analysis Points	40,000	488
Computation Time per point	0.04	0.08

Fig. 9. Experimental circuit

Table 2. Circuit Parameters

SiC-MOSFET	CMF20120D (Cree)
SiC-SBD	C2D10120 (Cree)
Gate Drive IC	HCPL3120 (Agilent)
Gate Resistor	0 Ω
Current Sensor	CWT1 (PEM)
DC Voltage E_d	500 V
Turn-Off Current i_D	70 A
Inductor L	2.0 mH

respectively. The three types of bus bars have the same PCB layout as shown in Fig. 11, although the line length ℓ and the distance d are different from each other. The upper layout of Fig. 11 shows the positive side of the DC voltage, and the lower layout is the negative side. The left side is connected to electrolytic capacitor and the right side is mounted to the SiC-MOSFET and SiC-SBD. A current sensor with a Rogowski coil is connected to the right side of the PCB.

5.3 Experimental Results Figs. 12(a) ~ (c) show experimental waveforms of v_{DS} and i_D when the MOSFET is turned off. In this case, dv/dt of v_{DS} reaches $50\text{ kV}/\mu\text{s}$, and di/dt of i_D becomes $3.1\text{ kA}/\mu\text{s}$. The peak voltages of the experimental results for bus bars I~III are almost the same voltage of about 800 V, because the stray inductances of the bus bars are the same value.

Table 3. Bus bar parameters

	t [mm]	w [mm]	ℓ [mm]	d [mm]
bus bar I	0.5	50	187.3	3.8
bus bar II	0.5	50	271.6	2.0
bus bar III	0.5	50	374.0	1.0

Fig. 10. Experimental setup of the chopper circuit

Fig. 11. PCB layout of the bus bar

Fig. 12. Experimental waveforms of v_{DS} and i_D when the MOSFET is turned off using bus bars I, II and III

These experimental results indicate that laminated bus bars having the same inductance can be designed using the specific inductance map.

5.4 Discussion of the Stray Inductance Table 4 shows the analysis and measurement results for the stray inductance of the bus bars, L_s . Here, L_{cal} is the result using the partial inductance method, and L_{TDR} shows the result for the bus bar inductance measured using TDR (Time Domain Reflectometry)⁽¹³⁾⁽¹⁴⁾. The measurement results for L_{TDR} correspond to the designed value, L_{cal} . In addition, the stray inductance L_s that is the sum of the DC-side inductance is derived from the peak voltage of v_{DS} and the current waveform di_D/dt , as follows,

$$L_s = -(818\text{ V} - 500\text{ V}) \cdot \frac{\mu\text{s}}{-3.12\text{ kA}} = 102\text{ nH} \dots\dots\dots (15)$$

Here, the L_s indicates the total stray inductance including ESL (Equivalent Series Inductance) of the electrolytic capacitor and the internal inductance of the power devices. Thus, the total stray inductance L_s is larger than the bus bar inductance L_{cal} .

6. Conclusion

This paper proposed high speed analysis methods for a symmetric bus bar structure and specific inductance searching method for a laminated bus bar. As a result, the computation time of the quarter analysis with PCG method is significantly lower compared with the conventional analysis. The quarter analysis of this paper is suitable for a laminated structure. In addition, the searching method is effective to reduce the computation time for drawing the inductance map. An asymmetry structure can also be applied to the conventional method and searching method. Moreover, the experimental results rated at 500 V and 70 A for a buck chopper circuit

Table 4. Analysis and measurement results for the stray inductance

	L_{cal} [nH]	L_{TDR} [nH]	L_s [nH]
bus bar I	40.3	42.9	107
bus bar II	38.5	41.1	115
bus bar III	36.2	37.3	102

using SiC-MOSFET and SiC-SBD confirm the usefulness of the design procedure.

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