Reverse-Blocking IGBTs with V-Groove Isolation Layer for Three-Level Power Converters

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Abstract

Multilevel power converters are among the most effective approaches to reduce power loss and to improve efficiency in power conversion systems. Reverse-blocking IGBTs (RB-IGBTs) have been improved and extended to higher breakdown voltage to be used as bidirectional switches in multilevel converter applications. In this work, a hybrid isolation process by combining thermal diffusion and V-Groove etching is developed to form 1200–1700-V RB-IGBTs. The details on 1700-V RB-IGBTs are presented in this paper. Compared with that of full diffusion, the thermal budget of the frontside surface deep boron diffusion has been reduced to less than one-third. Sufficient reverse-blocking capability and switching robustness have been successfully demonstrated. At the same switching loss level, on-state voltage of a 50 A-rated planar gate RB-IGBT is reduced to approximately 1.9 V compared with that of serially connected trench-gate field-stop IGBT (FS-IGBT) and free-wheeling diode (FWD). Experimental benchmarking on 1200-A module demonstrated that the energy loss in three-level inverter was reduced to 18% by using RB-IGBTs instead of IGBT and FWD pairs at typical switching frequencies for high-power, medium-voltage applications.

Keywords: RB-IGBT, three-level power converter, hybrid isolation process, thermal diffusion, V-groove

1. Introduction

Recently, various efforts have been made worldwide to reduce carbon dioxide emission. The main focus in the field of power electronics is the reduction of power loss and improvement of efficiency in power conversion systems. Multilevel power converters are among the most effective approaches to reduce both the switching loss and the size of the filters. Several types of neutral-point-clamped (NPC) three-level power converters have been proposed for renewable energy and uninterrupted power source (UPS) applications. Among them, the type using diodes to clamp the output to the neutral point has also been commercialized. However, these systems have the disadvantage of using a very large number of power semiconductor devices.

For solving the abovementioned problems, T-type NPC (T-NPC) three-level power converters with bidirectional switches as clamping devices have been proposed as shown in Fig. 1(a). Traditionally, the bidirectional switches are formed with serially connected insulated gate bipolar transistor (IGBT) and free-wheeling diode (FWD). Reverse-blocking IGBTs (RB-IGBTs), which were first developed for matrix converter applications, are well-suited for T-NPC inverters in order to reduce the total number of power devices and also the total loss by eliminating the diode from the conventional serial pair. A single-phase-leg circuit of a T-NPC inverter with bidirectional switches formed by anti-parallelized RB-IGBTs is shown in Fig. 1(b). We call this type of inverter as AT-NPC inverter.

However, RB-IGBTs tend to suffer low yield during fabrication when using the conventional thermal diffusion isolation process because of unusually high thermal budget. The isolation process along with the full V-groove process has been conceptually demonstrated. However, the fabricated structures become mechanically fragile during debonding for packaging.

We have recently made numerous efforts to improve both the device structures and the process technologies. Improvement in manufacturability has been attempted by combining emitter-side thermal diffusion and collector-side
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Anisotropic wet etching (V-groove etching) for 1200–1700-V RB-IGBTs. Our hybrid isolation process reduces the unusually high thermal budget in the wafer process and renders the RB-IGBT mechanically stable during the entire packaging process.

We compare the conventional full diffusion isolation process with our new hybrid process in Sects. 2 and 3. Using a 1700-V RB-IGBT as an example, we describe the electrical characteristics of the fabricated RB-IGBTs in Sect. 4. In Sect. 5, we provide the preliminary benchmark results to demonstrate the advantages of an AT-NPC three-level inverter using our 1700-V RB-IGBTs when compared with the conventional T-NPC inverter.

2. Overview of Conventional Isolation Process for RB-IGBTs

The edge termination structure of an RB-IGBT chip is schematically depicted in Fig. 2.

As shown in Fig. 2(a), our previous 1200-V RB-IGBT realizes its reverse blocking capability by extending the thermal budget used for 600-V devices to form a deeper (~200 µm) through-chip p⁺ isolation layer. Thermal diffusion occurs for a longer time at a high temperature. Since the diffusion depth increases with the square root of the diffusion time; it is difficult to extend the abovementioned full thermal diffusion process for higher-breakdown-voltage RB-IGBTs, which require a deeper isolation layer. Furthermore, lateral diffusion of the isolation layer also increases the die size. For higher-voltage devices, it is inappropriate to simply extend the deeper diffusion isolation process.

RB-IGBTs with isolation layers formed by V-groove etching through the entire silicon layer on backside of the wafer and subsequent ion implantation and activation on the surface of V-grooves have been demonstrated. However, this method has shortcomings in terms of both yield stability with regard to the large depth of the V-groove, and compatibility of the supporting substrate with the conventional backside metallization units.

3. Hybrid Isolation Process for RB-IGBTs

Fig. 2(b) shows the cross-sectional view of an RB-IGBT with the new isolation layer. The sequence of the device fabrication processes is as shown in Fig. 3. First, boron diffusion is conducted from the frontside of the wafer before the formation of surface cell structures. Second, after the thinning of the wafer backside, V-groove etching is performed from the backside until it crosses the boron diffusion layer. Third, boron is implanted into the wafer backside and the surface of the V-grooves. The collector layer is electrically connected to the frontside of the boron diffusion layer after boron activation. Finally, backside metallization is performed.

For higher-blocking-voltage devices, it is necessary to apply the hybrid isolation process. In addition to the advantage of shorter diffusion time, the yield loss associated with crystal defects in extremely high thermal budget has also been reasonably suppressed.

Figure 4 shows a cross-sectional scanning electron microscopy (SEM) image of a 1700-V RB-IGBT edge termination region on the wafer obtained before collector metallization (Fig. 3(c)). Excellent V-groove shape has been obtained. When compared with the thermal budget in the case of full diffusion in 1700-V devices, the thermal budget of the frontside surface deep boron diffusion has been significantly reduced to less than one-third in the hybrid scheme.
4. Electrical Characteristics of 1700 V RB-IGBT

The 1700-V RB-IGBT surface termination structure consists of field-plate flanked field limiting rings optimized for external charge immunity. The active region consists of striped planar gate cells with terraced gate oxide. With robust forward-blocking voltage and switching robustness maintained, the cell structure is optimized for the optimum on-state voltage (V_{on}). The vertical structure is a non-punch-through structure in order to achieve reverse blocking capability from the collector junction.

In the following section, the electrical characteristics of the RB-IGBTs are compared with those of the serially-connected field-stop IGBT (FS-IGBT) and FWD pair where applicable. The devices in comparison are neutral-point-clamping devices as shown in Fig. 1. All the devices (RB-IGBT, FS-IGBT, and FWD) exhibit a rated voltage of 1700 V and a rated current of 50 A.

4.1 Static Characteristics

The experimental off-state I-V characteristics at room temperature and at 125°C for a 50-A RB-IGBT are shown in Fig. 5. The forward-direction curves are measured at V_{GE} = 0 V, while the reverse direction curves are measured at V_{GE} = 15 V, for AT-NPC three-level applications. In terms of leakage current, the collector/n−base pn junction quality is as good as that of the frontside p-base/n−base junction. The on-state I-V characteristics of the RB-IGBT and the pair of trench-gated FS-IGBT and FWD are compared as shown in Fig. 6. The on-state voltage (V_{on}) of the RB-IGBT at 125°C is approximately 1.9 V lower at a rated current (I_{o}) of 50 A.

4.2 Switching Characteristics

4.2.1 IGBT Switching Characteristics

The relationships between the turn-off, turn-on, reverse recovery (RR) loss (E_{off}, E_{on}, E_{rr}) and V_{on} are compared as shown in Fig. 7. The bus voltage V_{DC} used in the experiments is 850 V. The aforementioned V_{on} reduction can be achieved at the same E_{off} level of the IGBT and FWD pair, while the E_{on} and E_{rr} are mildly sacrificed. The typical turn-off waveforms are shown in Fig. 8 for both the serially connected pair and the RB-IGBT at the same dV/dt of ~8 kV/µs.

4.2.2 Diode Reverse Recovery Performance

The RR waveforms for RB-IGBT at a rated current 50 A are shown in Fig. 9. The switching device is a 50-A 3.3-kV main switch IGBT (Fig. 1), which is our fifth-generation trench-gated FS-IGBT. The stray inductance (Ls) used in our test circuit is 0.3 µH. The external gate resistance of the IGBT is 1.6 Ω, and its turn-on dI/dt is 1.2 kA/µs.

Small (10% I_{o})-current RR waveforms are shown in Fig. 10 for two cases of IGBT turn-on dI/dt of 710 A/µs and 440 A/µs under the conditions of V_{DC} = 950 V, L_{s} = 0.8 µH, and T_{j} = 125°C. The external gate resistance is 5.8 Ω and 1.6 Ω for the two cases of dI/dt, respectively. There is no voltage spike at a current slew rate of less than 440 A/µs.

4.3 Switching Robustness

4.3.1 IGBT Robustness

The typical maximum current turn-off waveforms are shown in Fig. 11 under the conditions of I_{C} = 7 × I_{o}, V_{DC} = 1200 V, and L_{s} = 0.3 µH.
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Fig. 9. Reverse recovery waveforms at 50-A rated current

Fig. 10. Small-current reverse recovery waveforms corresponding to the two cases of IGBT turn-on \( \frac{di}{dt} \) of 710 A/\( \mu \)s and 440 A/\( \mu \)s. \( I_F = 5 \) A (10% \( I_0 \))

Fig. 11. Typical maximum current turn-off waveforms

The maximum \( \frac{dV}{dt} \) is approximately 10 kV/\( \mu \)s. The typical short-circuit safe operating area (SCSOA) waveforms are shown in Fig. 12. The non-destructive gate pulse width is 18 \( \mu \)s, and the bus voltage \( V_{DC} \) is 1200 V. Our RB-IGBT is robust enough to meet the application requirements.

4.3.2 Diode Reverse-recovery Robustness

Large (2\( \times \)\( I_0 \))-current RR waveforms are shown in Fig. 13 under the conditions of \( V_{DC} = 1200 \) V, \( L_s = 0.8 \mu \)H, \( R_{sw} = 20 \Omega \), and \( T_j = 125^\circ \)C. These waveforms are non-destructive (the test is not conducted towards destruction); the diode can sustain a peak power beyond 197 kW/cm\(^2\). The non-punched-through drift region and tuned injection efficiency contribute to the high ruggedness, although the collector junction depth is relatively thin when compared with the anode depth of the conventional FWD (5). It can also be inferred from the results that the shape of V-groove is not necessarily detrimental to the RR robustness.

5. Power Loss in AT-NPC Three-Level Inverter

The existing high-power module consists of 24 chips in parallel, as shown in Fig. 14, to form single 1200-A RB-IGBT module. The module structure is not optimized for RB-IGBTs. Two types of modules are formed using RB-IGBT chips at \( V_{on} = 3.1 \) V and \( V_{on} = 3.9 \) V, respectively, as shown in Fig. 7. These modules are henceforth denoted as RB-IGBT (A) and RB-IGBT (B), respectively. The switching losses are measured in the three-level inverter modes with the 1200-A 3.3-kV IGBT modules using our fifth-generation IGBT and FWD chipset. During the measurement, the case temperature is raised to 125\( ^\circ \)C, while the bus voltage is 900 V (\( V_{DC}/2 \) in Fig. 1), and the external gate resistance for all the IGBT modules is 3.3 \( \Omega \).

By using the experimental results, the three-level inverter power losses are calculated under the conditions of an output current of 400 A rms at 60 Hz, a power factor of 0.8, and a modulation ratio of 0.8, for two carrier frequencies (fc) of 500 Hz (a) and 1 kHz (b). The results are shown in Fig. 15. The RR loss (Err) in the RB-IGBT is closely coupled to
the turn-on loss (Eon) of the main IGBT. At high carrier frequency, reducing the Von in the RB-IGBT for lower Eon results in lower Eon in the main IGBT and, consequently, reduces the total power loss. It is beneficial to use RB-IGBT (A) when fc is 500 Hz and RB-IGBT (B) when fc is 1 kHz. For RB-IGBTs at fc = 500 Hz, as compared with the (IGBT+FWD) pair as NPC devices, the total power loss is reduced by 18% with RB-IGBT (A) modules, and by 16% with RB-IGBT (B) modules.

The carrier frequency of the IGBTs in high-power medium-voltage converters is -500 Hz [13]; therefore, the characteristics of our baseline chip are the same as those of RB-IGBT (A). The characteristics of RB-IGBT can also be instantly adjusted along the trade-off line shown in Fig. 7 in order to meet the requirements of the other applications.

6. Conclusion

We have developed a hybrid isolation process by combining thermal diffusion and V-groove etching for 1200–1700-V RB-IGBTs. Sufficient blocking capability and switching robustness have been successfully demonstrated for 1700-V devices. At the same switching loss level, the on-state voltage of the 50 A-rated planar-gate 1700-V RB-IGBT is reduced to approximately 1.9 V when compared with a serially connected trench-gate FS-IGBT and FWD.

At the typical carrier frequency of high-power medium-voltage applications, the experimental benchmarking on 1200-A module demonstrated that the energy loss in the three-level inverter is reduced by 18% when using RB-IGBTs instead of the IGBT and FWD pairs. It is now possible to reduce the power loss in high-power medium-voltage applications by adopting RB-IGBTs to form bidirectional switches.

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References

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