Analysis of Power Loss of Class E Amplifier with Nonlinear Shunt Capacitance

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(Manuscript received Feb. 13, 2013, revised July 10, 2013)

It is experimentally known that the efficiency of class E amplifiers deteriorates when the dc supply voltage is much lower than the designed value. However, the existing literature on efficiency and power loss analysis of class E amplifiers cannot explain the cause of this phenomenon at all. It is demonstrated in this paper that this deterioration of efficiency is caused by the influence of the nonlinearity of the output capacitance of the MOSFET. Owing to the nonlinearity of the output capacitance, the class E amplifier cannot achieve ZVS switching when dc supply voltage is lower than the designed value, even if the circuit is designed to achieve ZVS at the designed dc supply voltage. In this regard, this paper presents the power efficiency of the class E RF power amplifier as a function of dc supply voltage $V_{DD}$ when the shunt capacitance is nonlinear with the grading coefficient $m = 0.5$ as a representative value. With this modeling of the nonlinear shunt capacitance, non-ZVS switching at a low dc supply voltage can be reproduced with the theoretical waveforms, and the switching loss can be calculated at a dc supply voltage that is lower than the designed dc supply voltage. Then, the total power loss including the switching loss can be calculated. The result of the efficiency calculation demonstrates a deterioration of efficiency at low dc supply voltages as expected, and there was good agreement with the experimental results.

**Keywords:** class E power amplifier, power efficiency, non-linear shunt capacitance, switching loss, conduction loss, AM modulation

1. Introduction

In many applications of class E amplifiers, such as envelope elimination and restoration (1), amplitude shift keying (2), and amplitude modulation (3), the amplifier is operated with a varying dc supply voltage. One of the merits of using class E amplifiers in amplitude varying systems is their theoretically higher efficiency in the deep back-off region compared to linear power amplifiers. However, it has been experimentally shown (for example, by Thian (4)) that the efficiency of a class E amplifier deteriorates when the dc supply voltage is much lower than the originally designed supply voltage. Much research has been conducted on the efficiency of and power loss in class E amplifiers (5)-(9). In Ref. (5), Milosevic included the transistor on-resistance and equivalent series resistance (ESR) of $C_{DS}$ in his analysis. In Ref. (6), examined the ESR of a resonant inductive capacitive (LC) circuit as well. Reference (7) established the design equation of a class E amplifier by incorporating parasitic resistances, and Yang (6) extended this analysis to all duty ratios. Junqing (6) formulated new class E amplifier design equations to minimize power loss rather than achieve zero-voltage switching (ZVS) or zero-voltage slope switching (ZVSS). However, in all of these studies, the shunt capacitance of the class E amplifier was considered to be a linear capacitance, i.e., a constant capacitance; in such cases, the efficiency at a given dc supply voltage becomes a constant value, which removes the possibility of explaining the deterioration of efficiency at low dc supply voltages. In reality, the shunt capacitance of a class E amplifier is a combination of linear external and nonlinear transistor output capacitances (10)-(12). Especially in the high frequency domain, nonlinear output capacitance comes to dominate shunt capacitance (10)(12). Although the voltage and current in a class E amplifier are directly proportional to the dc supply voltage when the shunt capacitance is constant (13), this is not true when the shunt capacitance is nonlinear (4)(13). In Refs. (4) and (5), the nonlinear increment of output power versus dc supply voltage was demonstrated, and in Ref. (4), the deterioration of efficiency at low dc supply voltages was further determined from experimental results, although the mechanism underlying this efficiency deterioration was not explained. In Ref. (16), power efficiency was calculated numerically on the basis of the nonlinearity of shunt capacitance; however, the variation in efficiency corresponding to change in the dc supply voltage was not considered, and therefore, efficiency was not developed as a function of dc supply voltage. In Ref. (17), the power efficiency was also calculated numerically on the basis of the nonlinearity of shunt capacitance and shown to be a function of dc supply voltage. In Ref. (17), it was shown through simulation that the switch voltage waveform cannot achieve ZVS when the dc supply!  

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value, i.e., the dc supply voltage at which the class E amplifier achieves ZVS and ZVSS. However, only the on-resistance of the transistor and the switching loss were considered in that analysis, whereas conduction losses due to the parasitic resistances of other circuit elements were not incorporated. Thus, the percentage of influence of the switching loss was not clarified.

In this paper, the power efficiency of a class E amplifier with a nonlinear shunt capacitance is determined for dc supply voltages outside of the shunt’s design parameters. In the analysis, power loss due to a metal-oxide-semiconductor field-effect transistor (MOSFET) on-resistance, the series parasitic resistances of the series capacitance and inductance of the output LC filter, and the series parasitic resistance of the choke inductance are examined. On the basis of this, the power losses caused by individual parasitic resistances and nonzero voltage switching can be calculated. The results show that the switching loss dominates total power loss when the dc supply voltage is lower than the designed value. The contribution of this paper di

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where $\theta_d$ is the phase angle of the voltage at the body diode of the MOSFET when the MOSFET is turned on. Note that the maximum switch voltage is limited by the breakdown voltage of the MOSFET and in this analysis, $v_S$ is assumed to be lower than the breakdown voltage of the MOSFET. The analysis in this paper incorporates the fact that if a class E amplifier with nonlinear shunt capacitance is designed to achieve nominal operation at the designed dc supply voltage, it will not achieve ZVS operation at a dc supply voltage $V_{DD}$ lower than this designed value, as illustrated in Fig. 2. This phenomenon was explained in Ref. (17), and it is considered here because the equivalent shunt capacitance is high when the voltage across it is low. Therefore, it is assumed that the body diode turns on when $v_S$ drops below zero prior to switch turn-on when $V_{DD} > V_{DDdesigned}$, the designed value of the dc supply voltage. Otherwise, $v_S > 0$ at the instant of MOSFET switch turn-on, in which case $\theta_d$ is equivalently replaced with the switch turning-on time $\theta = \pi$. Therefore, the phase can be represented as $\theta_d < \pi$ when $V_{DD} > V_{DDdesigned}$ and $\theta_d = \pi$ when $V_{DD} \leq V_{DDdesigned}$.

This paper examines the circuit behavior of a class E amplifier outside of its designed conditions, particularly with respect to variation in the dc supply voltage. The equations that follow are formulated by incorporating the three assumptions listed above. Because the dc voltage drop across the choke inductance is zero and the current through the choke inductor is constant, the following condition is satisfied:

$$V_{DD} - r_{LRFC} I_{DD} = \frac{1}{2\pi} \int_0^{2\pi} v_S d\theta$$

Because only the fundamental frequency component is extracted from the switch voltage waveform $v_S$ by the output band-pass filter, the real part of the fundamental frequency component of the switch voltage $v_S$ is equal to the voltage amplitude across the load resistance, parasitic resistance of series capacitor $C_f$, and parasitic resistance of series inductor, $L_f$:

$$\left( R + r_{CF} + r_{LF} \right) I_m = \frac{1}{\pi} \int_0^{2\pi} v_S \sin(\theta + \phi) d\theta$$

The imaginary part of the fundamental component of the switch voltage is equal to the fundamental component of the voltage across the reactance of the output $L_f C_f$ circuit, and it is given by

$$\xi_I = \frac{1}{\pi} \int_0^{2\pi} v_S \cos(\theta + \phi) d\theta$$

where

$$\xi = \omega L_f = \frac{1}{\omega C_f}$$

By substituting (8) into (9)–(11) and solving the three equations, solutions for three unknown variables $I_{DD}$, $I_m$, and $\phi$ are obtained. To solve this associated equation, a numerical method is invoked because the equation is transcendental.

3. Power Losses and Efficiency

3.1 Power Loss Due to Parasitic Resistances

The power loss due to the MOSFET on-resistance is obtained as

$$P_{ONloss} = \frac{1}{2\pi} \int_{\theta_d}^{2\pi} r_S i_S^2 d\theta$$

The MOSFET on-resistance $r_S$ can be calculated as a ratio of the drain source voltage to the drain source current. In the triode region, the drain source current is expressed as

$$i_{DS} = K (v_{GS} - V_T) v_{DS}$$

where $V_T$ is the MOSFET threshold voltage, and $K (A/V^2)$ is the MOSFET transconductance coefficient, which is determined by the chip layout and the fabrication process and defined as

$$K = \mu_n C_{ox}\frac{W}{L}$$

where $\mu_n$ is the electron mobility, $C_{ox}$ is the oxide capacitance, $W$ is the channel width, and $L$ is the channel length. Note that the above equation is valid if $v_{GS} \ll v_{DS}$ is satisfied. Where “$\ll$” means here that the right hand side is more than ten times greater than the left hand side. If the MOSFET is driven with a typical rectangular voltage signal, $v_{DS}$ is at a constant level (such as 5 V) during the ON period, whereas the drain-source voltage is at a very low level (such as 0.1 V). Hence, if the MOSFET is driven by a typical rectangular signal, the on-resistance can be regarded as a constant value given by

$$r_S = \frac{1}{K (v_{GS} - V_T)}$$

The power loss due to the ESR of $C_{ds}$ is obtained as

$$P_{ESRloss} = \frac{1}{2\pi} \int_0^{\theta_d} r_{ESR} C_r^2 v_S^2 d\theta$$

The power loss due to the parasitic resistance of the choke inductor is obtained as

$$P_{LRFCloss} = \frac{1}{2\pi} \int_0^{2\pi} r_{LRFC} I_{LRFC}^2 d\theta$$

The power loss due to the parasitic resistances of the series inductor and capacitor is obtained as

$$P_{CFLloss} = \frac{1}{4\pi} \int_0^{2\pi} \left( r_C + r_L \right) I_m^2 d\theta$$
3.2 Switching Loss  

The switching loss can be obtained as the time average of energy charged in the shunt capacitance at the instant of switch turn-on. The switch voltage at the instance of switch turn-on is obtained as

\[
v_{SO\text{N}} = \begin{cases} 
V_{bi} \left( \frac{I_{DD} \pi - 2I_m \cos \phi}{2V_{bi} \omega C_j} + 1 \right) - 1 & V_{DD} \leq V_{DD\text{designed}} \\
0 & V_{DD} > V_{DD\text{designed}}
\end{cases}
\]

Energy charge in the shunt capacitance at the instance of switch turn-on is then

\[
W = \int_{v_{SO\text{N}}}^{0} C_{1\text{VS}} dv_S
= \int_{v_{SO\text{N}}}^{0} \frac{C_{1\text{VS}} v_S}{\sqrt{1 + \frac{v_S}{V_{bi}}}} dv_S
\]

and switching loss is obtained as

\[
P_{SW\text{loss}} = \frac{W}{T}
\]

3.3 Power Losses  
The total power loss is sum of all the above power losses such as the switching loss and the power losses caused by the parasitic resistances. Hence, it is described as

\[
P_{\text{total}} = P_{ON\text{loss}} + P_{ESR\text{loss}} + P_{RFC\text{loss}} + P_{C\text{fL\text{loss}}} + P_{SW\text{loss}}
\]

The total power loss is the difference between \( P_{\text{in}} \) and \( P_{\text{out}} \)

\[
P_{\text{loss}} = P_{\text{in}} - P_{\text{out}}
\]

The power efficiency is obtained as
4. Calculation Example and Its Verification

The test specifications of the class E amplifier parameters were \( V_{DD} = 20 \, \text{V} \), \( f = 4 \, \text{MHz} \), and \( R = 67 \, \Omega \), and a nonlinear shunt capacitance with \( V_{bi} = 0.7 \, \text{V} \) was assumed. On the basis of these specifications, the circuit parameters were designed using equations shown in Ref. (4), resulting in \( C_{\beta 0} = 400 \, \text{pF} \), \( L_f = 26.7 \, \mu\text{H} \), and \( C_f = 67.9 \, \text{pF} \). For the experiment, an IRF510 power MOSFET was used as a transistor switch; according to its SPICE model, its parameters were designed using equations shown in Ref. (4), resulting in \( r_s = 0.26 \, \Omega \), \( r_L = 0.5 \, \Omega \), and \( r_C = 0.01 \, \Omega \). As the circuit could not achieve nominal operation at \( f = 4 \, \text{MHz} \), some of the parameters were modified to achieve nominal operation, and by setting \( f = 3.83 \, \text{MHz} \), \( R = 50.5 \, \Omega \), \( C_{\beta 0} = 400 \, \text{pF} \), \( V_{bi} = 0.77 \, \text{V} \), \( m = 0.5 \), \( L_f = 26.7 \, \mu\text{H} \), and \( C_f = 67.9 \, \text{pF} \), the circuit was able to achieve ZVS and ZVSS operation. Under these conditions and on the basis of the measured values of the parasitic resistances shown above, we solved the associated equations (9)–(11) using Mathcad, a numerical program. Figure 3 shows the theoretical waveforms of switch voltage \( V_S \) obtained through Mathcad calculation. It is seen that \( V_S \) is achieved ZVS at \( V_{DD} = 30 \) and \( 20 \, \text{V} \) but, not at \( V_{DD} = 5 \, \text{V} \). Figure 4 shows observed waveforms of the switch voltage \( V_S \) and output voltage \( v_o \); this confirms the results of Fig. 3, i.e., that ZVS was achieved at \( V_{DD} = 30 \) and \( 20 \, \text{V} \) but not at \( 5 \, \text{V} \). Figure 5 shows the measured efficiency and the theoretical efficiency, \( \eta_{\text{loss}} \), at \( r_s = 0, 0.26 \) and \( 0.5 \, \Omega \). As Mathcad did not converge for \( V_{DD} \) less than 2.5 \, \text{V} \), only experimental data were available in this region; however, as shown in Fig. 5, the experimental results show close agreement with theory. It is seen from the figure that approximately 10\% power was lost in the radio frequency choke coil; otherwise, efficiency deteriorated at \( V_{DD} < 5 \, \text{V} \), a deterioration pattern that closely followed theoretical calculation. Finally, it can be seen from Fig. 5 that the effect of the value of \( r_S \) is not large, with any differences mostly falling within the measurement error range.

\[
\eta_{\text{loss}} = \frac{P_{\text{out}} - P_{\text{loss}}}{P_{\text{in}}} \tag{25}
\]

\[
\frac{V_{DD}}{V_{in}} = \frac{f}{2f_{\text{osc}}} = \frac{r_s}{2r_L} \tag{26}
\]

\[
\begin{align*}
\text{plots of output voltage and input current. The output of the function generator was a rectangular wave with four Vp-p and a 1.4-V offset. The on-resistance of the IRF510 MOSFET was estimated to be } r_S = 0.26 \, \Omega \text{ by inserting the SPICE model transconductance coefficient of } K = 2.48 \text{ and the value of the output of the function generator into (15). As the on-resistance of a MOSFET varies significantly with drain current and temperature, its exact value could not be estimated from a SPICE model or data sheet; therefore, a rough estimation of a representative value was used for calculation. The parasitic parameter values were measured experimentally as follows: } r_{\text{LBFC}} = 8 \, \Omega, r_{C1} = 0.5 \, \Omega, r_{L} = 0.5 \, \Omega, \text{ and } r_{Cf} = 0.01 \, \Omega. \text{ As the circuit could not achieve nominal operation at } f = 4 \, \text{MHz} \text{, some of the parameters were modified to achieve nominal operation, and by setting } f = 3.83 \, \text{MHz}, R = 50.5 \, \Omega, C_{\beta 0} = 400 \, \text{pF}, V_{bi} = 0.77 \, \text{V}, m = 0.5, L_f = 26.7 \, \mu\text{H}, \text{ and } C_f = 67.9 \, \text{pF}, \text{ the circuit was able to achieve ZVS and ZVSS operation. Under these conditions and on the basis of the measured values of the parasitic resistances shown above, we solved the associated equations (9)–(11) using Mathcad, a numerical program. Figure 3 shows the theoretical waveforms of switch voltage } V_S \text{ obtained through Mathcad calculation. It is seen that } V_S \text{ is achieved ZVS at } V_{DD} = 30 \text{ and } 20 \, \text{V} \text{ but, not at } V_{DD} = 5 \, \text{V}. \text{ Figure 4 shows observed waveforms of the switch voltage } V_S \text{ and output voltage } v_o; \text{ this confirms the results of Fig. 3, i.e., that ZVS was achieved at } V_{DD} = 30 \text{ and } 20 \, \text{V} \text{ but not at } 5 \, \text{V}. \text{ Figure 5 shows the measured efficiency and the theoretical efficiency, } \eta_{\text{loss}}, \text{ at } r_s = 0, 0.26 \text{ and } 0.5 \, \Omega. \text{ As Mathcad did not converge for } V_{DD} \text{ less than } 2.5 \, \text{V}, \text{ only experimental data were available in this region; however, as shown in Fig. 5, the experimental results show close agreement with theory. It is seen from the figure that approximately } 10\% \text{ power was lost in the radio frequency choke coil; otherwise, efficiency deteriorated at } V_{DD} < 5 \, \text{V}, \text{ a deterioration pattern that closely followed theoretical calculation. Finally, it can be seen from Fig. 5 that the effect of the value of } r_S \text{ is not large, with any differences mostly falling within the measurement error range.}
\end{align*}
\]
5. Discussion

The efficiency of the class E amplifier as measured using a linear shunt capacitance was generally constant versus dc supply voltage but degraded when the dc supply voltage was very low. This was mainly caused by the nonlinear effects of the shunt capacitance. Figure 6 shows estimated values of switching and other conduction losses as the dc supply voltage was changed. Note that in these calculations, it was assumed that $rL_{RFC} = rC_1 = rC_f = rL_f = 0 \Omega$ in order to eliminate the influence of any resistance other than the on-resistance. As seen in the figure, the switching loss became high when $V_{DD} < V_{DD\text{designed}}$; this is because ZVS was not achieved below the designed voltage. In designing amplitude-varying systems in which the power amplifier essentially has a high peak-to-average power ratio, this nonlinear effect should be taken into account. Although a class E amplifier would ideally not be designed to be operated below a designated dc supply voltage, the deterioration of efficiency at low dc supply voltages is relatively minor, as shown in Fig. 5, where even the lowest efficiency is over 70% owing to the fact that the switching loss was much lower than the conduction loss in the frequency range shown (Fig. 6).

One method of avoiding efficiency deterioration is to design a class E amplifier that can take the lowest possible dc supply voltage; if this is done, the amplifier will be able to achieve ZVS in the form of off-nominal operation and a high efficiency can be obtained at higher dc supply voltages.

6. Conclusions

In this study, the power efficiency of a class E amplifier was calculated under the assumption that power loss in the low-supply voltage-region is caused by the nonlinearity of MOSFET output capacitance. The calculated efficiency closely matched experimental results in cases where the supply voltage was either lower or higher than the designed value. Furthermore, analysis of the observed waveform confirmed the assumption that non-ZVS conditions occur when $V_{DD} < V_{DD\text{designed}}$. When the supply voltage was between half and full design voltage, there was insignificant deterioration of efficiency, a result that can be explained by the insignificant switching loss in this region. The deterioration of efficiency only became significant at supply voltages lower than half of the designed voltage; again, this occurred because the switching loss becomes significant in this region.

Acknowledgment

This work was supported by JSPS KAKENHI Grant Numbers 24360153, 25820112, and funds (No.:127005) from the Central Research Institute of Fukuoka University.

References

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