Output Ripple Minimization of Single-Stage Power-Factor-Correction Bidirectional Buck AC/DC Converter

Balaji Veerasamy* Student Member, Wataru Kitagawa* Member
Takaharu Takeshita*^{a)} Senior Member

(Manuscript received Aug. 11, 2014, revised Oct. 27, 2014)

This paper presents a PWM control method for a variable-voltage single-stage bidirectional buck AC/DC converter for suppressing the output voltage ripple with a high source power factor. The proposed method maintains the minimum number of commutations during the control period for realizing three voltage levels close to the output reference voltage. The overall loss of the converter is reduced using the proposed method, which is verified experimentally.

Keywords: Single-stage, AC/DC converter, pulse width modulation, power factor control, output ripple

1. Introduction

Increasing number of battery storage devices and solar panels interacting with the grid needs high efficient converters to utilize the maximum power from such sources. Efficient single-stage bidirectional AC/DC converters are replacing the conventional two-stage converters for their compact size and simple control methods for renewable and energy saving technologies. Switching power electronic converters employs Pulse Width Modulation (PWM) method for converting the AC voltage to a desired DC voltage. Several single-stage isolated AC/DC converters^{(1)–(7)} are developed for buck operation mode mainly achieved through a transformer, which finally increases the overall size of the converter system. Ripple minimization is an important feature of single-stage non-isolated PWM controlled converters⁽⁸⁾ with a limited input phase control range is proposed with reduced number of commutations during the control period for reduced DC ripple. As power factor regulations are required to meet the standards, switching patterns⁽⁹⁾⁽¹⁰⁾ are developed to improve the source power factor by controlling the input current of the converter. However the input power factor range is improved by phase shifting, the control method⁽¹⁰⁾ cannot maintain a low output DC ripple. The main drawback of this control method is the high variation of output voltage, producing an increased voltage stress on the output capacitor leading to a high ripple on the DC voltage.

In this paper, additional PWM switching methods are proposed to reduce the output DC ripple by limiting the high variation of output voltage. Additionally the proposed method increases the efficiency of the converter by reducing the overall loss in the circuit. This paper is organized as follows: Sections 2 presents the basic control system and analytical model of the single-stage buck AC/DC converter, Section

3 describes the proposed PWM switching methods which is compared with the conventional single-stage PWM switching methods. Sections 4 discusses the input supply phase control and finally the experimental results are discussed with comparing the proposed and conventional methods.

2. Proposed Circuit and Its Operating Principle

2.1 Converter Configuration and Analytical Model

Figure 1 shows the single-stage bidirectional buck AC/DC converter system. The three phase AC source voltages e_{su} , e_{sv} and e_{sw} are converted to a constant desired DC voltage V_{dc} through the six bidirectional IGBT switches $S_{up} - S_{wn}$. The bidirectional operation is achieved by reverse blocking IGBTs or connecting two IGBTs in series reverse. The circuit has two LC filters on both the input side and the output side. The input filter reactor L_f , capacitor C_f and resistor R_f are connected to the voltage source to suppress the outflow of the harmonic current. The output filter smoothing reactor L and capacitor C are connected to the output side of the converter for suppressing the output voltage ripple caused by PWM switching. The input current references i_u^* , i_v^* and i_w^* (* denotes reference) of the converter are selected so as to

Fig. 1. Single-Stage Bidirectional AC/DC Converter

a) Correspondence to: Takaharu Takeshita. E-mail: take@nitech.ac.jp

* Graduate School of Engineering, Nagoya Institute of Technology
Gokiso, Showa, Nagoya 466-855, Japan

realize unity power factor between the source currents i_{su} , i_{sv} and i_{sw} and corresponding source voltages e_{su} , e_{sv} and e_{sw} . The switching patterns of switches $S_{up} - S_{wn}$ are controlled so as to obtain a desired output voltage with realizing an unity source power factor through two PI controllers and the input phase detector as shown in Fig. 1.

A symmetrical three-phase source voltages e_{su} , e_{sv} and e_{sw} with an effective line voltage E are expressed in (1). The input voltages e_u , e_v and e_w are approximately equal to the source voltage by ignoring the voltage drop across inductor L .

$$\begin{bmatrix} e_{su} \\ e_{sv} \\ e_{sw} \end{bmatrix} \approx \begin{bmatrix} e_u \\ e_v \\ e_w \end{bmatrix} = \sqrt{\frac{2}{3}}E \begin{bmatrix} \cos \theta \\ \cos(\theta - 2\pi/3) \\ \cos(\theta + 2\pi/3) \end{bmatrix} \dots \dots \dots (1)$$

The input current references are expressed in terms of its effective value I^* and power factor angle φ^* in (2).

$$\begin{bmatrix} i_u^* \\ i_v^* \\ i_w^* \end{bmatrix} = \sqrt{2}I^* \begin{bmatrix} \cos(\theta + \varphi^*) \\ \cos(\theta + \varphi^* - 2\pi/3) \\ \cos(\theta + \varphi^* + 2\pi/3) \end{bmatrix} \dots \dots \dots (2)$$

The input instantaneous power p_{in} is given in (3) terms of input voltages and input current references in (1) and (2).

$$p_{in} = e_u i_u^* + e_v i_v^* + e_w i_w^* \dots \dots \dots (3)$$

The output instantaneous electric power p_{out} is given in (4) using the output voltage reference V_c^* and the output current I_{dc} .

$$p_{out} = V_c^* I_{dc} \dots \dots \dots (4)$$

The input effective current reference I^* is obtained by balancing the input and output instantaneous powers from (3) and (4).

$$I^* = \frac{V_c^* I_{dc}}{\sqrt{2}\{e_u \cos(\theta + \varphi^*) + e_v \cos(\theta + \varphi^* - \frac{2\pi}{3}) + e_w \cos(\theta + \varphi^* + \frac{2\pi}{3})\}} \dots \dots \dots (5)$$

3. Analysis of PWM Methods

3.1 Basic Principle of Duty Cycles Figure 2 shows the converter model without the input and output filters for calculating the duty cycles. The duty cycles of the six switches $S_{up} - S_{wn}$ during the control period are denoted by $d_{up} - d_{wn}$, respectively. The control period T_s of the circuit is very short when compared with the time constant of the circuit. The main feature of the principle PWM method is reduced number of commutations during the control period and two switches are not conducting during the control period T_s . In order to ensure continuous output current and preventing short circuit of input line voltages, only one among the three switches on each output phase should be conducting during the control period. Therefore, the following relationship of duty cycles are obtained.

$$d_{up} + d_{vp} + d_{wp} = 1 \dots \dots \dots (6)$$

$$d_{un} + d_{vn} + d_{wn} = 1 \dots \dots \dots (7)$$

The input current references i_u^* , i_v^* and i_w^* are given in terms of the duty cycles and expressed in the following equations.

Fig. 2. Converter model

Fig. 3. Switching patterns and waveforms of principle PWM control

$$i_u^* = (d_{up} - d_{un})I_{dc} \dots \dots \dots (8)$$

$$i_v^* = (d_{vp} - d_{vn})I_{dc} \dots \dots \dots (9)$$

$$i_w^* = (d_{wp} - d_{wn})I_{dc} \dots \dots \dots (10)$$

The average output voltage for each control period is obtained as follows, and is equal to output voltage reference V_c^* .

$$V_c^* = (d_{up} - d_{un})e_u + (d_{vp} - d_{vn})e_v + (d_{wp} - d_{wn})e_w \dots \dots \dots (11)$$

3.2 Principle PWM Strategy Figure 3 shows the input current references, duty cycles and output voltage waveforms of the principle PWM method for an input phase interval of $0 \leq \theta < \pi/3$. The input current references i_u^* , i_v^* and i_w^* are the highest (H), intermediate (M) and lowest (L) ($i_u^* > i_v^* > i_w^*$) with the input phase reference $\varphi^* = 0$. Figure 3(a) shows the output waveforms when the voltage reference V_c^* is high and Fig. 3(b) shows the output waveforms when the voltage reference V_c^* is low. In both the cases the output phase p is commutated between the phase u of the maximum input current reference i_u^* and the phase v of the intermediate input current reference i_v^* and the output phase n is commutated between the phase v of the intermediate input current reference i_v^* and the phase w of the minimum input

current reference i_w^* . Therefore, only two commutations appear during the control period and thus the duty cycles of two switches are zero.

$$d_{wp} = 0, d_{un} = 0 \dots \dots \dots (12)$$

The duty cycles of the conducting switches are obtained from (8)–(10) and (12).

$$\left. \begin{aligned} d_{up} &= \frac{i_u^*}{I_{dc}}, & d_{vp} &= 1 - \frac{i_u^*}{I_{dc}} \\ d_{vn} &= 1 + \frac{i_w^*}{I_{dc}}, & d_{wn} &= -\frac{i_w^*}{I_{dc}} \end{aligned} \right\} \dots \dots \dots (13)$$

As shown in Fig. 3, the switching patterns are obtained by comparing the input current references i_u^* , i_v^* and i_w^* with the triangular carriers T_p and T_n . The positive triangular carrier T_p varies between 0 and I_{dc} , the negative triangular carrier T_n varies between 0 and $-I_{dc}$ and both the triangular carriers are in phase with each other. In order to realize the duty cycles of the four switches conducting during the control period as given in (13) the positive switch S_{up} is turned on when $i_u^* \geq T_p$ and conducts till the positive switch S_{vp} is turned on when $i_u^* \leq T_p$. Similarly when $i_w^* \leq T_n$ the negative switch S_{wn} is turned on and conducts till the negative switch S_{vn} is turned on when $i_w^* \geq T_n$. From this switching method the output voltage waveform V_c consists of three positive voltage levels e_{uv} , e_{uw} and e_{vw} for realizing a high voltage reference V_c^* as shown in Fig. 3(a). In Fig. 3(b) the output voltage wave consists of two voltages e_{uv} , e_{vw} and a zero voltage to realize the low output voltage reference V_c^* . Therefore, the output phase p is not connected to the minimum input phase and output phase n is not connected to the maximum input phase. Because of this condition the switching loss and noise is reduced in the converter.

The threshold voltage value V_{cth}^* is an output voltage reference point between the high output voltage reference and low output voltage reference. The output voltage references is stated to be low when it is less than the threshold voltage V_{cth}^* which consists of a zero voltage during each control period. At the threshold value under $0 \leq \theta \leq \pi/3$, the duty cycles d_{up} and d_{vn} are equal at which both the positive and negative switches are commutated at the same time. Therefore from this condition of the duty cycles, the following relationship is obtained from (13).

$$\frac{i_u^*}{I_{dc}} = 1 + \frac{i_w^*}{I_{dc}} \dots \dots \dots (14)$$

The input current references i_u^* and i_w^* are expressed in terms of the effective current reference I^* and the following equality is obtained from (2).

$$\frac{\sqrt{2}I^* \cos(\theta + \varphi^*)}{I_{dc}} = 1 + \frac{\sqrt{2}I^* \cos(\theta + \varphi^* + 2\pi/3)}{I_{dc}} \dots \dots \dots (15)$$

By using Eqs. (1), (5) and (15) the threshold output reference voltage V_{cth}^* is obtained as,

$$V_{cth}^* = \frac{E \cos \varphi^*}{\sqrt{2} \cos(\theta + \varphi^* - \pi/6)} \quad (0 \leq \theta \leq \pi/3) \dots \dots (16)$$

From the above equation the threshold output voltage V_{cth}^*

Fig. 4. Principle PWM control ($\varphi^* = 0$)

Table 1. Duty cycles of six patterns

Pattern	Reference			Duty cycles					
	H	M	L	d_{up}	d_{vp}	d_{wp}	d_{un}	d_{vn}	d_{wn}
I	i_u^*	i_v^*	i_w^*	$\frac{i_u^*}{I_{dc}}$	$1 - \frac{i_u^*}{I_{dc}}$	0	0	$1 + \frac{i_w^*}{I_{dc}}$	$-\frac{i_w^*}{I_{dc}}$
II	i_v^*	i_u^*	i_w^*	$1 - \frac{i_v^*}{I_{dc}}$	$\frac{i_v^*}{I_{dc}}$	0	$1 + \frac{i_w^*}{I_{dc}}$	0	$-\frac{i_w^*}{I_{dc}}$
III	i_v^*	i_w^*	i_u^*	0	$\frac{i_v^*}{I_{dc}}$	$1 - \frac{i_v^*}{I_{dc}}$	$-\frac{i_u^*}{I_{dc}}$	0	$1 + \frac{i_u^*}{I_{dc}}$
IV	i_w^*	i_v^*	i_u^*	0	$1 - \frac{i_w^*}{I_{dc}}$	$\frac{i_w^*}{I_{dc}}$	$-\frac{i_u^*}{I_{dc}}$	$1 + \frac{i_u^*}{I_{dc}}$	0
V	i_w^*	i_u^*	i_v^*	$1 - \frac{i_w^*}{I_{dc}}$	0	$\frac{i_w^*}{I_{dc}}$	$1 + \frac{i_v^*}{I_{dc}}$	$-\frac{i_v^*}{I_{dc}}$	0
VI	i_u^*	i_w^*	i_v^*	$\frac{i_u^*}{I_{dc}}$	0	$1 - \frac{i_u^*}{I_{dc}}$	0	$-\frac{i_v^*}{I_{dc}}$	$1 + \frac{i_v^*}{I_{dc}}$

depends upon the values of θ , φ^* and E . Under the input phase condition $\varphi^* = 0$, the threshold voltage V_{cth}^* is the minimum value of $E/\sqrt{2}$ at $\theta = \pi/6$ and the maximum value of $\sqrt{2}E/\sqrt{3}$ at $\theta = 0, \pi/3$.

The input phase pattern changes for every $\pi/3$ of the input current references i_u^* , i_v^* and i_w^* , and therefore six patterns (represented as I–VI) occur for a single cycle of three phase source. Figure 4 shows the waveforms of source voltage, input current references and output voltage waveforms for a single cycle of three phase source with the principle control method. Figures 4(a) and (b) show the principle PWM control of all the six patterns for the high and low output voltage reference V_c^* , respectively where the output voltage has three positive voltage levels for high voltage reference and two positive and a zero voltage to realize low output voltage. The expansion of the highlighted portion of Figs. 4(a) and (b) are shown in Figs. 3(a) and (b), respectively when the input phase condition is $e_u > e_v > e_w$. Table 1 summarizes the duty cycles for the six patterns I–VI where two duty cycles are zero in each pattern thus reducing the ripple on the DC voltage.

The PWM control method has restrictions towards the input phase angle φ^* with limits of the control range of $-\pi/6 \leq \varphi^* \leq \pi/6$ and $5\pi/6 \leq \varphi^* \leq 7\pi/6$ (8).

3.3 Conventional PWM Strategy for Power Factor Control

Two switching strategies for improving the control ranges of the input phase reference φ^* between $-\pi/2 \leq$

Fig. 5. PWM control for power factor control

Fig. 6. Partial waveforms of conventional method

$\varphi^* \leq -\pi/6$ and $\pi/6 \leq \varphi^* \leq \pi/2$ are introduced for achieving high input power factor control⁽¹⁰⁾. Figures 5(a) and (b) show the input currents reference, duty cycles and output voltage waveforms of two conventional switching patterns for the input phase reference of $\varphi^* = -\pi/3$ and $\varphi^* = \pi/3$, respectively. The duty cycles are realized with respect to the level of input reference current so the output phase p is commutated between the maximum input current reference and intermediate input current reference and output phase n is commutated between the intermediate input current reference and minimum input current reference.

Figures 6(a) and (b) show the partial waveforms of input current references and output voltage waveforms in highlighted portions of Figs. 5(a) and (b), respectively. As shown in Fig. 6(a), during the input voltage phase condition ($e_u > e_v > e_w$) when the order of the input current reference is $i_u^* > i_w^* > i_v^*$ and the duty cycles are realized with respect

to the level of input reference current so the output phase p is commutated between the maximum input current reference i_u^* and intermediate input current reference i_w^* and output phase n is commutated between the intermediate input current reference i_w^* and minimum input current reference i_v^* . The duty cycles ($d_{up} - d_{wn}$) of the switches $S_{up} - S_{wn}$ during $0 < \theta < \pi/3$ are given in (17) according to pattern VI.

$$\left. \begin{aligned} d_{up} &= \frac{i_u^*}{I_{dc}}, \quad d_{vp} = 0, \quad d_{wp} = 1 - \frac{i_u^*}{I_{dc}} \\ d_{un} &= 0, \quad d_{vn} = -\frac{i_v^*}{I_{dc}}, \quad d_{wn} = 1 + \frac{i_v^*}{I_{dc}} \end{aligned} \right\} \dots \dots (17)$$

In order to realize the duty cycles of four switches conducting during the control period as obtained in (17), the input current references are compared with the triangular carriers. When $i_u^* \geq T_p$ the positive switch S_{up} is turned on and conducts till the positive switch S_{vp} is turned on when $i_u^* \leq T_p$. Similarly when $i_w^* \leq T_n$ the negative switch S_{wn} is turned on and conducts till the negative switch S_{vn} is turned on when $i_w^* \geq T_n$. As a result three voltages e_{uw} , e_{uv} and e_{vw} appears on the output of the converter during the control period. Because of this switching method the minimum voltage phase w is connected to output phase p and maximum voltage phase u connected to the output phase n . Therefore during the control period, two positive and one negative voltages appear on the output voltage V_c of the converter to realize a low output reference voltage V_c^* . The negative voltage gradually increases and reaches maximum when one of the line voltage is zero. Similarly Fig. 6(b) shows the waveforms of input reference current and output waveforms for a leading input reference of $\varphi^* = \pi/3$ during the input voltage phase condition ($e_u > e_v > e_w$).

The conventional method for improving the power factor increases the ripple on the output voltage as the small output voltage reference V_c^* is realized with three voltages varying between the positive and negative line voltages.

3.4 Proposed PWM Strategy for Power Factor Control

The principle control method of this converter is maintaining two commutations during each control period to reduce the ripple on the DC voltage, but during the power factor control for low output voltage reference the ripple on the DC voltage is increased due to high variation of output voltage V_c between maximum and minimum line values to realize low voltage reference V_c^* . Therefore, ultimate goal of the proposed method is to reduce the output DC ripple by limiting the high voltage variation on the output voltage V_c . Figure 7 shows the input current references, duty cycles and output voltage waveforms of the proposed PWM control method for two control ranges $-\pi/2 \leq \varphi^* \leq -\pi/6$ and $\pi/6 \leq \varphi^* \leq \pi/2$ under same conditions in Fig. 5. In both the patterns the low reference voltage V_c^* is realized with positive, zero and negative voltages on the output voltage V_c close to the voltage reference V_c^* and without a maximum negative voltage in order to reduce the ripple. In conventional method the two carrier waves T_p and T_n are in phase with each other whereas in the proposed method the carrier waves T_p and T_n are out of phase with each other.

Figures 8(a) and (b) show the partial waveforms of input reference currents, duty cycles and output voltage of highlighted portions of Figs. 7(a) and (b), respectively.

Fig. 7. Proposed PWM control

Fig. 8. Partial waveforms of proposed method

Figure 8(a) shows the waveforms of input reference currents, duty cycles and output waveforms for a lagging input reference of $\varphi^* = -\pi/3$. During the input voltage phase condition ($e_u > e_v > e_w$), the order of the input current reference is $i_u^* > i_w^* > i_v^*$. The output phase p is commutated between the phase u of the maximum input current reference i_u^* and the phase v of the intermediate input current reference i_w^* and the output phase n is commutated between the phase v of the minimum input current reference i_v^* and the phase w of the intermediate input current reference i_w^* . Thus the duty cycles of the switches are same as given in (17) but only the position of the commutation is shifted. The input current references are compared with the triangular carrier in order to obtain the switching patterns. When $i_u^* \geq T_p$ the positive switch S_{up} is turned on and conducts till the positive switch S_{vp} is turned on when $i_u^* \leq T_p$. Similarly when $i_w^* \leq T_n$ the negative switch S_{wn} is turned on and conducts till the negative switch S_{vn} is turned on when $i_w^* \geq T_n$. As a result positive line voltage e_{uv} , negative line voltage e_{vw} and zero appears on the output of the converter during the control period. The value of the neg-

Fig. 9. U-phase equivalent circuit and vector diagram

ative line voltage is close to the reference voltage and never reaches the maximum voltage value.

Similarly Fig. 8(b) shows the method for obtaining the switching patterns from input current reference and triangular carrier for a leading input reference of $\varphi^* = \pi/3$ during the input condition ($e_u > e_v > e_w$). And in the proposed method the input current i_u consists of current pulses with the same sign as the input current reference which can reduce the harmonics of the switching frequency. As a result the input filter loss is reduced. Similarly the output filter loss is reduced due to the minimization of the ripple thus reducing the overall loss of the converter.

4. Input Supply Phase Control

The current flowing in the input filter generates a phase difference between the source current i_{su} and the input current to the converter i_u . Figure 9(a) shows the equivalent circuit of the input phase u and Fig. 9(b) shows the vector diagram of the fundamental wave. The phase of the input current reference i_u^* is controlled by changing the input power factor reference φ^* to achieve unity source power factor.

From Fig. 9(a) the input current i_u^* is obtained from the source current i_{su} and reactive current through capacitor i_{cu} .

$$i_u^* = i_{su} - i_{cu} = I_p - jI_q \quad (18)$$

The input active current I_p is expressed in (19)

$$I_p = \frac{V_c^* i_{dc}}{\sqrt{3}E} \quad (19)$$

The reactive current I_q flowing in the capacitor can be obtained from the effective value of E of the source line voltage.

$$I_q = \frac{E/\sqrt{3}}{-\omega L_f + \frac{1}{\omega C_f}} = i_{cu} \quad (20)$$

Input power factor reference φ^* is obtained using the active current I_p and reactive current I_q from (19) and (20), respectively and is given in (21).

$$\varphi^* = \tan^{-1} \frac{-I_q}{I_p} \quad (21)$$

5. Results and Discussions

5.1 Experimental Conditions Figure 10 shows the experimental configuration and Table 2 lists the experimental specifications with the source voltage of 200 V and 60 Hz, and with a constant resistive load. Figures 11, 12 and 13 show the source voltage e_{su} , source current i_{su} , input current i_u , output voltage V_c and DC voltage V_{dc} of the principle PWM, conventional and the proposed PWM strategies,

Fig. 10. Experimental configuration

Table 2. Experimental condition

Source voltage E, ω	200 V, $2\pi \times 60$ rad/s
DC voltage reference V_{dc}^*	160 V, 80 V
Output power P_{out}	1 kW
Input filter L_f, C_f, R_f	1.0 mH, 10.47 μ F, 47 Ω
Load R	26 Ω
Inductance L	20 mH
Capacitor C	1500 μ F
Carrier frequency f_s	10 kHz

Fig. 11. Overall waveforms by principle PWM method

Fig. 12. Overall waveforms by conventional method

respectively when the DC voltage reference V_{dc}^* is changed from 160 V to 80 V with a source phase voltage of 200 V and 60 Hz. In Fig.11, for high output voltage reference $V_{dc}^* = 160$ V, the output voltage V_c have only positive voltages to

Fig. 13. Overall waveforms by proposed method

Fig. 14. Partial waveforms of principle PWM method

realize the output DC voltage. For low output voltage reference $V_{dc}^* = 80$ V, the output voltage V_c have positive and zero voltages. The input phase reference $\varphi^* = -24^\circ$ for $V_{dc}^* = 160$ V which is in the limit of control of principle PWM method ($-\pi/6 \leq \varphi^* \leq \pi/6$). But in the case of low output voltage reference $V_{dc}^* = 80$ V the input phase reference $\varphi^* = -64^\circ$ which is out of the principle control range so a maximum input phase reference of $\varphi^* = -30^\circ$ is given. As shown in Fig. 12, in the conventional power factor improvement method, the input phase reference φ^* is shifted by an angle of -64° for maintaining unity source power factor when the voltage reference $V_{dc}^* = 80$ V so in this condition the output voltage V_c varies between maximum and minimum line voltages. But in the case proposed PWM method as shown in Fig. 13, the output voltage V_c varies between positive line voltage and a small negative line voltage.

Figures 14, 15 and 16 show the partial waveforms of source voltage e_{su} , source current i_{su} , input current i_u , output voltage V_c and DC voltage V_{dc} of Figs. 11, 12 and 13, respectively when the output voltage reference $V_{dc}^* = 80$ V. In principle PWM control method the source voltage e_{su} and source current i_{su} are not in phase as shown in Fig. 14 due to the maximum input phase reference of $\varphi^* = -30^\circ$. The input current i_u is in phase with the source voltage e_{su} . In the conventional method as shown in Fig. 15, the input current i_u is shifted to an input phase reference of $\varphi^* = -64^\circ$ to bring the source current i_{su} in phase with its corresponding voltage. The conventional method generates high ripple when the output voltage waveform reaches maximum negative value

Fig. 15. Partial waveforms of conventional method

Fig. 16. Partial waveforms of proposed method

when one of the line voltage is zero. In the proposed method as shown in Fig. 16, the source current i_{su} is in phase with the corresponding source voltage e_{su} as the input current i_u is shifted to a phase reference φ^* equal to -64° . In case of the proposed method the output voltage waveform never reaches maximum negative line voltage and because of this condition the ripple on the DC voltage is low. When comparing the waveform of the input current i_u between the methods, the proposed method can reduce the harmonics of the switching frequency component of the input current as the input current waveforms consist of current pulses with the same sign as the input current reference.

Figure 17 shows the data analysis of input power factor $\cos \varphi_s$ versus the output/input voltage ratio V_c^*/E . A high power factor is achieved for high voltage output profiles by the power factor control method when compared to the principle PWM control method. Even though the power factor control method satisfies unity power factor but at small output-input voltage ratios the leading current caused by the LC filter cannot be completely compensated causing low level power factors. But this problem is not associated with light load conditions as the source current is also low.

5.2 Ripple Analysis Figure 18 shows the partial waveforms of the output voltage V_c and DC voltage V_{dc} for a output voltage reference of $V_{dc}^* = 80$ V. In the conventional PWM strategy a negative voltage appearing during every control period and its level increases when one of line voltage is approaching zero, so the ripple on the DC voltage is 0.45 V, whereas in the proposed PWM strategy the output voltage V_c

Fig. 17. Input source power factor control

Fig. 18. Output waveforms comparison

Fig. 19. Ripple analysis of input current of converter and output voltage

has three voltages levels including the zero voltage and the minimum negative voltage so reducing the ripple to 0.1 V, which is four times less than the ripple caused by the conventional method. Figures 19(a) and (b) show the harmonic spectrum of the input current i_u , output voltage V_c and DC voltage V_{dc} of conventional and proposed control methods, respectively, where the input fundamental component and the DC voltage are 100% under DC voltage reference V_{dc}^* of 80 V. For the conventional pattern the percentage of input current

Table 3. Power loss analysis under $V_{dc}^* = 80$ V

Control scheme	Output Power P_{out} [W]	Input filter Loss P_{if} [W]	Converter Loss P_c [W]	Output filter Loss P_{of} [W]	Overall Loss P_{ol} [W]
Conventional	246.160	0.48	8.59	1.41	10.48
Proposed	246.123	0.402	6.39	1.306	8.09

Fig. 20. Input filter, converter and output filter loss comparison between conventional and proposed methods

harmonics at the carrier frequency $\omega_c = 2\pi \times 10$ krad/s is 45%. But for the proposed pattern the input current harmonics is reduced to 23% as the input current waveforms contains current pulses of same sign as the input current reference. In the frequency analysis, the ripple caused by the conventional method and the proposed control method at carrier frequency are 120.2% and 49.5%, respectively. The DC voltage ripple at carrier frequency caused by the conventional method and the proposed control method are 0.0084% and 0.0066%, respectively. Therefore the output voltage ripple and DC voltage ripple have been reduced by 58.18% and 21.42%, respectively by proposed PWM strategy by preventing high negative line voltage to appear on the output voltage of the converter.

5.3 Loss Analysis and Total Power Factor The comparison of losses between the conventional and proposed PWM strategies are calculated using the power meter Yokogawa WT 3000. Table 3 compares the input filter loss P_{if} , converter loss P_c and output filter loss P_{of} of conventional method with the proposed method for an output voltage reference of 80 V. As shown in Table 3, the proposed method reduces the overall losses by 20% for a low output power P_{out} of 246 W.

Figure 20 shows the analysis of the input filter loss P_{if} , converter loss P_c and output filter loss P_{of} of the two strategies for various output voltage values from 60 V to 120 V and finally concluding that the proposed method reduces all the losses compared to that of the conventional method.

Figure 21 compares the total power of the three methods with respect to the output DC voltage of the converter. Conventional method improves the total power factor when compared to the principle PWM method. But the proposed method shows improvement in total power factor than the conventional method as the supply current harmonics are reduced.

Fig. 21. Total Power Factor

6. Conclusion

This paper presents a PWM method for a single-stage bidirectional buck AC/DC converter for reducing the output voltage ripple by controlling the negative voltage level on the output side of the converter. The converter also maintains the high input power factor range and reduces the input current harmonics. The efficiency of the converter system is improved by reducing the overall losses and the effectiveness is verified using the experimental results.

Acknowledgement

This study is supported in a part by Power Academy Japan Grant-in-Aid for Exploratory Research (doctoral student frame) 2013-14, "Development of single stage bidirectional AC/DC converter for battery charging system", and we express our gratitude to all the persons concerned.

References

- (1) M. Daniele, P.K. Jain, and G. Joos: "A Single-Stage Power-Factor-Corrected AC/DC Converter", *IEEE Trans. Power Electron.*, Vol.14, No.6, pp.1046–1055 (1999)
- (2) Q. Zhao, F.C. Lee, and F.S. Tsai: "Voltage and Current Stress Reduction in Single-Stage Power Factor Correction AC/DC Converters With Bulk Capacitor Voltage Feedback", *IEEE Trans. Power Electron.*, Vol.17, No.4, pp.477–484 (2002)
- (3) W.Y. Choi and J.S. Yoo: "A Bridgeless Single-Stage Half-Bridge AC/DC Converter", *IEEE Trans. Power Electron.*, Vol.26, No.12, pp.3884–95 (2011)
- (4) M.S. Agamy and P.K. Jain: "An Adaptive Energy Storage Technique for Efficiency Improvement of Single-Stage Three-Level Resonant AC/DC Converters", *IEEE Trans. Ind. Electron.*, Vol.47, No.1, pp.176–184 (2011)
- (5) S.K. Ki and D. Lu: "A High Step-Down Transformerless Single-Stage Single-Switch AC/DC Converter", *IEEE Trans. on Power Electron.*, Vol.28, pp.36–45 (2013)
- (6) D.S. Wijeratne and G. Moschopoulos: "A Comparative study of Two Buck-Type Three-Phase Single-Stage AC-DC Full-Bridge Converters", *IEEE Trans. Power Electron.*, Vol.29, No.4, pp.1632–1645 (2014)
- (7) Y. Hu, L. Huber, and M.M. Jovanovic: "Single-Stage, Universal-Input AC/DC LED Driver with Current-Controlled Variable PFC Boost Inductor", *IEEE Trans. on Power Electron.*, Vol.27, pp.1579–98 (2012)
- (8) Y. Onoe, W. Kitagawa, and T. Takeshita: "PWM Strategy of Bi-directional Buck AC/DC Converter for suppressing Output Voltage Ripple", 2011 Annual Conference of IEEE, Industry Applications Society (2011)
- (9) S. Ishikawa and T. Takeshita: "Input Power Factor Control of Three-Phase to Three-Phase Matrix Converters", *IEEE Trans. IA*, Vol.178, No.3, pp.42–52 (2012)
- (10) B. Veerasamy, W. Kitagawa, and T. Takeshita: "Input Power Factor Control of Bi-directional AC/DC Converter", 2013 IEEE International conference on Power Electronics and Drives (PEDS), pp.1103–1108 (2013)

Balaji Veerasamy (Student Member) was born in Tamilnadu, India in 1985. He completed the B.E. and M.E. degree in electrical and electronics engineering from Anna University, India in 2006 and 2008, respectively. He is presently working towards his doctor degree in Nagoya Institute of Technology. His research interest is on single-stage AC/DC converter for renewable applications.

Takaharu Takeshita (Senior Member) was born in Aichi, Japan in 1959. He received the B.S. and M.S. degrees in electrical engineering from the Nagoya Institute of Technology, Nagoya, Japan, in 1982 and 1984, respectively, and the Ph.D. degree from Nagoya University, Nagoya, Japan, in 1990. Since 1991, he has been with the Nagoya Institute of Technology, where he is currently a full professor and is engaged in research on power converter system and motor control. He is a member of SICE, SSPRTJ, IEIEJ and IEEE.

Wataru Kitagawa (Member) was born in Japan in 1977. He completed the B.E. and M.E. degree in faculty of electrical engineering from Doshisha University in 2000 and 2002, respectively. He joined IBM Japan in April 2002 and later joined Lenovo Japan in January 2006. He completed his Ph.D. degree in March 2009 from Doshisha University. From April 2010 he is working as assistant professor in Nagoya Institute of Technology and his area of interest is numerical analysis of electromagnetic field.