This paper presents a novel single-phase inverter equipped with a buck-boost-type power decoupling function that is suitable for PV generation. The proposed buck-boost-type power decoupling circuit relaxes the increase of the DC-bus voltage of the PWM inverter compared with the conventional boost-type power decoupling circuit. This prevents the increase in switching and conduction losses caused by the high voltage rating switching devices. Another feature of the proposed inverter is a power decoupling control method based on a single-phase p-q theory. Because the proposed power decoupling method reduces the low-frequency ripple current flowing at the DC input, the electrolytic DC-bus capacitor is replaced by a small film capacitor that has a longer lifetime. The effectiveness of the proposed system is verified through simulation and experiments using a 200 W experimental setup.

Keywords: power conditioner, power decoupling, buck-boost chopper

1. Introduction

In recent years, interest in photovoltaic (PV) power generation systems has grown among power electronics engineers because of the current environmental issues. Tremendous kind of inverter topologies and control methods have been proposed(1)–(4). In particular, in a single-phase inverter system, power pulsation with twice the grid frequency appears at the dc input terminal. This results in improper control of the maximum power point tracking (MPPT) of the PV modules as shown in Fig. 1.

In order to reduce the voltage fluctuation at the input dc-bus caused by the pulsed power, electrolytic capacitors with large capacitance have been connected to the dc-bus. This method is called passive power decoupling (PPD), and most of the power conditioners on the market have applied the PPD method. However, the lifetime of electrolytic capacitors is relatively short, and it is shortened further when used under a high atmospheric temperature conditions. Hence, a serious breakdown may occur due to the short electrolytic capacitor lifetime. The lifetime of the PV panel has been extended to more than 20 years owing to technical innovation. However, most of the power conditioners may not work for more than 20 years without maintenance. So, it is necessary to extend the lifetime of the power conditioner in order to recover the initial cost of the PV power generation systems. Of course, we may be able to use film capacitors instead of the large electrolytic capacitors with the PPD method; however, the volume of the power conditioner must increase because the volume of the film capacitor is more than 20 times larger than that of the electrolytic capacitor. In order to solve the abovementioned problems, an active power decoupling (APD) concept for a single-phase utility interactive inverter/converter, which can reduce the pulsed power in the input dc capacitors, has been proposed(5)–(17). A distinctive feature of the APD concept is that the pulsed energy is stored in an additional decoupling capacitor with large voltage fluctuation. A typical example of the power decoupling circuit utilizing a boost-chopper circuit is shown in Fig. 2. However, due to the voltage boosting operation of the APD circuit, dc-bus voltage at the PWM inverter is increased and switching devices with high voltage ratings have to be used. Hence, the switching loss and conduction loss of the switching devices are increased, and the conversion efficiency of the power conditioner cannot be improved.

In order to overcome this defect, this paper proposes a novel APD circuit and its control method, which provides high conversion efficiency. In the proposed APD circuit, both the buck-boost-type APD circuit and the direct power transfer function are applied. The buck-boost-type APD circuit enables storage of the pulsed energy in the APD capacitor with a minimum increase in the dc-bus voltage at the inverter portion. Hence, the volume of the APD capacitor can be reduced, and the loss of the PWM inverter circuit can also be reduced. The direct transfer function of the APD circuit reduces the power loss of the APD circuit. Owing to the above
contributions, high conversion efficiency and long lifetime of the power conditioner can be realized.

This paper first describes the circuit configuration and the operation principle of the proposed power conditioner. Next, a novel control method based on a single-phase p-q theory that the authors have proposed is explained. Finally, the effectiveness of the proposed method is verified through simulation and experiment.

2. Main Circuit Configuration and Operation Principle

Figure 3 shows main circuit configuration of the proposed power conditioner with a buck-boost-type APD circuit. Table 1 shows the parameters of the proposed circuit. In order to confirm the basic performance of the proposed circuit, grid voltage, \( V_{AC} \), of 100 Vrms and the dc input voltage, \( V_{CDC} \), of 200 V is applied in this study. MPPT control has yet to been applied to the inverter, but any of the MPPT control method could be applied to this APD circuit as conventional PV inverters.

The proposed inverter circuit is composed of a conventional single-phase PWM inverter and an APD circuit which is indicated by the dotted line. The APD circuit is composed of switching devices, \( S_{X1}, S_{X2}, S_{X3}, S_{X4} \), a small film capacitors, \( C_{X} \), inductor \( L_{X} \), and diodes \( D_{X}, D_{G1}, D_{G2} \). \( R_{DC} \) of 2 \( \Omega \) is used to simulate the voltage droop characteristics of the PV module. In the case when the grid voltage and output current of the inverter are given by Eqs. (1) and (2), the instantaneous output power of the power conditioner is given by Eq. (3),

\[
v_{AC} = V_{AC} \cos \omega t \\
i_{AC} = I_{AC} \cos \omega t \\
p_{AC} = \frac{1}{2}V_{AC}I_{AC} + \frac{1}{2}V_{AC}I_{AC} \cos 2\omega t
\]

where \( V_{AC} \) is the peak value of the grid voltage, \( I_{AC} \) is the peak value of the inverter output current, and \( \omega \) is the grid angular frequency. The second term in Eq. (3) is the pulsed instantaneous power, \( p_{AC} \), as shown in Eq. (4).

\[
p_{AC} = \frac{1}{2}V_{AC}I_{AC} \cos 2\omega t
\]

In order to make the dc input power, \( p_{DC} \), constant, Eq. (5) have to be satisfied.

\[
p_{DC} = V_{CDC}I_{DC} = \frac{1}{2}V_{AC}I_{AC}
\]
voltage, $v_X$, of the power decoupling capacitor increases.

On Mode II, the ac output power, $p_{AC}$, is larger than the dc input power, $p_{DC}$, and the power flow on Mode II is expressed as Fig. 5(b). Since the dc input power, $p_{DC}$, needs to be kept constant, required power for ac output is supplied both from the dc input voltage, $V_{DC}$, and the decoupling capacitor, $C_X$. A part of the required energy is supplied from the dc input voltage when switch $S_{X2}$ is turned off, and the additional energy required for the ac output power is supplied directly from the decoupling capacitor through switch $S_{X2}$. The stored energy in the decoupling capacitor is supplied directly to the PWM inverter, the loss caused by power transmission can be reduced, and hence, high conversion efficiency of the power conditioner can be realized.

The additional switches, $S_{X3}$ and $S_{X4}$, are turned off when switch $S_{X2}$ is turned on. When the decoupling capacitor voltage, $v_X$, is higher than that of the dc input voltage, $V_{DC}$, the off-state additional switches, $S_{X3}$ and $S_{X4}$, prevent the backflow of the current from the decoupling capacitor to the input dc power source. When the decoupling capacitor voltage, $v_X$, is lower than the dc input voltage, $V_{DC}$, the off-state additional switches enables the diode, $D_{G1}$, to conduct and to supply the current from the decoupling capacitor, $C_X$, to the inverter. The additional switches of $S_{X3}$ and $S_{X4}$ are turned on and off at the same time in order to reduce the conduction losses of these switches.

### 3. Required Capacitance and Operating Voltage of the Decoupling Capacitor

In order to store the pulsed power, $p_{rip}$, of the single-phase inverter to the power decoupling capacitor, the stored power, $p_C$, on the decoupling capacitor needs to have the same value as the pulsed instantaneous power, $p_{rip}$, as shown in Eq. (7).

$$C_X v_X \frac{dv_X}{dt} = -\frac{1}{2} V_{AC} I_{AC} \cos 2\omega t \quad \cdots \quad (7)$$

The pulsed voltage appearing in the decoupling capacitor is expressed as,

$$v_X (t) = \sqrt{\frac{V_{AC} I_{AC}}{2\omega C_X}} \sin 2\omega t + V^2_X \quad \cdots \quad (8)$$

where $V^*_X$ is the dc-biased voltage of the decoupling capacitor.

Figure 6(a) shows an example of the voltage waveforms in the boost-type power decoupling circuit. The minimum voltage of the decoupling capacitor, $V_{Xmin1}$, in the boost-type power decoupling circuit is given by Eq. (9), and it must be higher than the input voltage, $V_{DC}$. And, the maximum voltage, $V_{Xmax1}$, and the average voltage command, $V^*_X$, of the decoupling capacitor are given by Eqs. (10) and (11), respectively.

$$V_{Xmin1} = \sqrt{V_{AC} I_{AC} + V^2_X} \geq V_{DC} \quad \cdots \quad (9)$$

$$V_{Xmax1} = \sqrt{V_{AC} I_{AC} + V^2_X} \quad \cdots \quad (10)$$

$$V^*_X \geq \sqrt{\frac{V_{AC} I_{AC}}{2\omega C_X} + V^2_{CDC}} \quad \cdots \quad (11)$$

Figure 7(a) shows the relationship between the voltage and the capacitance of the decoupling capacitor in the boost-type power decoupling circuit in the case when the dc input voltage is $V_{DC} = 200$ V, the grid voltage is $V_{AC} = 100 \sqrt{2}$ V, and the ac output power is $p_{AC} = 1$ kW. Here, $V_{Xmax}$, $V_{Xmin}$, and $V^*_X$ represent the maximum voltage, the minimum voltage, and the dc-biased voltage of the decoupling capacitor, respectively. The decoupling capacitance $C_X$ should be determined by considering the maximum volume of the decoupling capacitor and the voltage rating of the MOSFET used in the PWM inverter. For example, when the decoupling capacitance of $50 \mu$F is used, the maximum voltage appearing
at the dc-bus of the PWM inverter reaches 410 V. It is difficult to use the MOSFETs with voltage rating of 600 V on this operating condition.

Figure 6(b) shows an example of the voltage waveforms in the buck-boost-type power decoupling circuit. In this case, the power decoupling capacitor voltage \( V_{CDC} \) at the dc-bus of the PWM inverter reaches 370 V. It is difficult to use the MOSFETs with voltage rating of 600 V or less can be used very safely, and also, the switching loss of the power device can also be reduced.

It should be noted that maximum voltage of the power decoupling capacitor in the boost-type power decoupling circuit is increased with increase of the dc input voltage. On the other hand, the maximum voltage of the power decoupling capacitor in the buck-boost-type power decoupling circuit does not increase even if the dc input voltage, \( V_{CDC} \), is increased.

In general, generation voltage of the photovoltaic module changes with the load condition and the irradiation condition. In the case when the input voltage is increased to \( V_{CDC} = 300 \) V, maximum voltage of the decoupling capacitor in the boost-type power decoupling circuit increases to 466 V, though the maximum voltage of the decoupling capacitor in the buck-boost-type remains 370 V. Therefore, the power devices with higher voltage rating must be used in the boost-type power decoupling circuit.

4. Control Method

Figure 8 shows a block diagram of the control circuit, which is composed of the PLL control, the ac current control, and the power decoupling control.

4.1 Control of Power Decoupling Circuit

In order to ensure accurate control of the power decoupling circuit, accurate calculation of the pulsed instantaneous power, \( p_{trip} \), which is given by Eq. (4), is important.

In order to calculate the pulsed power, \( p_{trip} \), the single-phase p-q theory that the authors have already proposed is used. A feature of the single-phase p-q theory is that the instantaneous reactive and the effective power are calculated on the rotating d-q coordinate that is synchronized with the grid voltage.

In order to perform the d-q transformation shown in Eq. (16), it is necessary to know two values for the stationary coordinate: \( v_{\alpha} \) and \( v_{\beta} \).

\[
\begin{bmatrix}
\begin{align*}
|v_\alpha| & = \cos(\omega t) & \sin(\omega t) \\
|v_\beta| & = -\sin(\omega t) & \cos(\omega t)
\end{align*}
\end{bmatrix}
\]

However, two orthogonal values for single-phase power cannot be defined from a single-phase voltage or current. In this theory, the real voltage of the grid voltage \( V_{AC} \) is defined as the orthogonal value of \( v_{\alpha} \) on the \( \alpha \)-axis. Also, the other orthogonal value of \( v_{\beta} \) on the \( \beta \)-axis is given as a virtual value. Since the rotating coordinate needs to synchronize with the grid voltage, a PLL circuit as shown in Fig. 9 is used.

Figure 9 shows the voltage and current values of the single-phase inverter and the virtual voltage and current vectors on the rotating coordinate. In the PLL circuit, an estimated virtual value for \( v_{\beta} \) is generated using the following equation:

\[
v_{\beta} = v_\alpha \sin(\omega t) = V_{AC} \sin(\omega t)
\]
Hence, we could detect the peak amplitude of the grid voltage, \( V_{AC} \), which can be detected from the d-axis value, \( v_d \).

Since the inverter current, \( i_{AC} \), is controlled to synchronize with the grid voltage, \( v_{AC} \), the current amplitude, \( I_{AC} \), appears on the d-axis value, \( i_d \), in the rotating coordinate system. Once we obtain the voltage and current values on the d-q coordinate, the instantaneous pulsed power, \( p_{rip} \), is given from Eq. (4).

Block diagram of the power decoupling control is shown in the upper side of the Fig. 8. The power decoupling control circuit is composed of current control for the decoupling inductor, \( i_{X1} \), and average voltage control for the decoupling capacitor, \( v_X \). Hence, the inductor current command, \( i_{X1}^* \), is given by

\[
i_{X1}^* = \frac{p_{rip}}{V_{CDC}} = \frac{v_d i_d}{2V_{CDC}} \cos 2\omega t, \quad \cdots \cdots \cdots \cdots \cdots (18)
\]

The dc bias voltage control command, \( V_X^* \), for the decoupling capacitor is added to the power decoupling control command. The dc bias voltage of the decoupling capacitor is adjusted so that the minimum voltage, \( V_{Xmin} \), of the decoupling capacitor does not reduce lower than the grid voltage, \( V_{CDC} \), and the maximum voltage, \( V_{Xmax} \), of the decoupling capacitor does not exceed the voltage rating of the MOSFETs.

4.2 Output Current Control

In order to realize the functions of both the sinusoidal ac output current generation and the power decoupling, the PWM signal is modified from the conventional one. Figure 10 shows the modulation signal and the resultant switching pattern when the output current is positive. The switches, \( S_1 \) and \( S_2 \), of one phase-leg of the inverter are driven by the pulse-width modulated signal with the carrier frequency of 20 kHz, and the switches, \( S_3 \) and \( S_4 \), of the other phase-leg are triggered by 180 degree pulses with the grid frequency of 50 Hz in order to convert the polarity of the output current. Switch \( S_4 \) turns on and \( S_3 \) turns off while the output current is positive, so their switching losses and switching noises are reduced. The gate signals of these switches are generated based on the mode control signal (Modes I and II). The mode control signal is generated by the comparator using the pulsed instantaneous power, \( p_{rip} \), as shown in Fig. 8.

On Mode I, the switches of \( S_{X3} \) and \( S_{X4} \) are kept to on-state, and required output power is supplied from only the input power source. Hence, the output current control and the modulation of the PWM inverter are performed in the same manner with a conventional PWM inverter. The modulation...
signal, \( \lambda(t) \), for the switches \( S_1 \) and \( S_2 \) is calculated by Eq. (19).

\[
\lambda(t) = \frac{V_{AC} \cos \omega t}{V_{CDC}} \quad \text{............... (19)}
\]

The gate signal of switch \( S_1 \) and the pulse waveform appearing at the output terminal voltage, \( v_{VIN} \), of the inverter are shown in Fig. 11(a). Surplus of the input current supplied from the dc input power source is stored in the power decoupling capacitor and hence the dc input current is maintained to a constant value.

On Mode II, output power is supplied alternatively from the dc input terminal and power decoupling capacitor, while keeping the dc input power constant. In order that short circuit between dc input and power decoupling capacitor does not occur, either \( S_{X2} \) or \( S_{X3} \) and \( S_{X4} \) are turned on. In order to realize the above requirement, the time sharing modulation method is applied.

On the first stage, switches \( S_1, S_4, S_{X3}, \) and \( S_{X4} \) are turned on, whereas switch \( S_{X2} \) is kept off-state, and the output power is supplied from the dc input power source. On the conventional PWM inverter, the current flowing from the dc input power source, \( i_{DC} \), fluctuates and is expressed as Eq. (20).

\[
i_{DC}(t) = \frac{V_{AC} + I_{AC}}{2V_{CDC}} (1 + \cos 2\omega t) \quad \text{............... (20)}
\]

In order to realize a constant dc current input, the modulation signal, \( \lambda_{DC}(t) \), for switch \( S_1 \) is given by Eq. (21).

\[
\lambda_{DC}(t) = \frac{\lambda(t)}{1 + \cos 2\omega t} \quad \text{............... (21)}
\]

Hence, the resultant dc input current is given by Eq. (22).

\[
i_{DC} = \frac{V_{AC} + I_{AC}}{2V_{CDC}} \quad \text{............... (22)}
\]

Another required output power is supplied from the decoupling capacitor by turning the switch \( S_{X2} \) on while \( S_{X3} \) and \( S_{X4} \) are turned off. Since the decoupling capacitor voltage, \( v_X \), is not same with the input voltage, \( V_{CDC} \), the original modulation signal, \( \lambda(t) \), is modified based on the ratio of dc input voltage \( V_{CDC} \) to the decoupling capacitor voltage \( v_X \), and the modified modulation signal, \( \lambda_{X2}(t) \), for \( S_{X2} \) is given by Eq. (23).

\[
\lambda_{X2}(t) = (\lambda(t) - \lambda_{DC}(t)) \times \frac{V_{CDC}}{v_X} + \lambda_{DC}(t) \quad \text{............... (23)}
\]

Hence, the gate signal of the switch \( S_{X2} \) and the resultant pulse waveform that appeared in the output terminal voltage, \( v_{VIN} \), of the inverter are shown in Fig. 11(b).

The turn off loss and surge voltage appearing on the switch \( S_{X2} \) are suppressed since the switch \( S_{X2} \) turns off just after the turn on of the switch \( S_1 \). But the turn on loss of the switch \( S_{X2} \) occurs in the same manner as a conventional PWM inverter. Based on the above design, the control block diagram of the output current is shown in Fig. 12.

5. Simulation and Experimental Result

Table 2 shows the parameter of the control circuit. Low pass filters, LPF1, LPF3, LPF5, and LPF7 are used for extracting the dc component from the input signal, and the cut-off frequency is set to 3 Hz. And low pass filters, LPF2, LPF4, and LPF6, are used for reducing the switching frequency component from the input signal, and the cut-off frequency is set to 1000 Hz. Control parameters of each PI controller are determined experimentally so that the output current and the power decoupling is reasonably controlled.

Figures 13(a) and (b) shows the simulated results for both the inactive and active condition of the proposed power decoupling method, respectively, where the input voltage is \( V_{CDC} = 200 \) V, the grid voltage is \( \omega = 100 \) Vrms, and the output power is \( p_{AC} = 200 \) W. In order to observe the buck-boost operation of the power decoupling circuit when APD function is activated, the control command for the average voltage of the decoupling capacitor, \( V_{X} \), is set to 200 V, which is same value as dc input voltage, \( V_{CDC} \). When the power decoupling circuit is inactive, the pulsed current of 2.2 A appears in the dc input current, \( i_{DC} \). However, when the APD function is activated, the pulsed current is reduced to 0.5 A. A large voltage pulsation with twice the grid frequency appears in the decoupling capacitor voltage, \( v_X \). This means that the pulsed power caused by the ac output power is...
transferred to the power decoupling capacitor. In addition, the decoupling capacitor voltage reduces to below the dc-bus voltage. This means that we can use lower voltage ratings for the power devices.

Figures 14(a) and (b) shows the experimental results for both the inactive and active conditions of the power decoupling method, respectively. The pulsated current component contained in the dc input current, \( i_{dc} \), is reduced after the APD function, although small amount of the ripple current still remains. This is because the gain of the power decoupling control portion cannot be set higher due to the time delay of the DSP controller. Hence, it can be reduced when high speed controller is applied. As shown in Figs. 14(a) and (b), the total harmonic distortion (THD) of the grid current \( i_{out} \) without APD condition is 2.6% and that with APD condition is 3.2%.

Figure 15 shows the conversion efficiency of the experimental setup. In the case when the APD circuit is disconnected from the experimental setup, the conversion efficiency reaches to 96% at 200 W output. In the case when the power decoupling circuit is activated, the conversion efficiency is 94.3% at 200 W output. Decrease in conversion efficiency caused by the operation of the proposed APD circuit is less than 2%. This value is smaller than that of the conventional power decoupling circuit, and would be acceptable drawback in increasing the lifetime of the power converter.

6. Conclusions

This paper presented a novel single-phase inverter with a buck-boost-type power decoupling function and its control method. The proposed control method provides a low ripple current at the dc input portion without large electrolytic capacitor, and THD of the output current is sufficient to connect to the grid. In addition, the proposed power decoupling circuit can reduce losses of the inverter by applying switching devices with lower voltage rating, compared to the conventional circuit. The effectiveness of the proposed system is verified through the experimental setup.

References


Single-phase Power Conditioner with a Power Decoupling Circuit (Shota Yamaguchi et al.)


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