Load Current Distribution between Parallel Inverters based on Capacitor Voltage Control for UPS Applications

Mohammad Bani Shamseh∗ Non-member, Teruo Yoshino∗∗ Fellow
Atsuo Kawamura∗ Fellow

(Manuscript received Aug. 19, 2016, revised March 16, 2017)

Many challenges are encountered when uninterruptible power supply (UPS) modules are operated in parallel to meet the power demand of the load. The circulating current is one prominent example of these challenges that may cause serious damage to equipment. Hence, control algorithms must ensure that the current is shared equally or in proportion to the power ratings of the parallel inverters, while mitigating the circulating current. Another challenge is that all parallel inverters should have equal output voltage, phase, and frequency. This paper proposes a new method to control parallel UPS modules. The method is based on regulating the capacitor voltage of the \textit{LCL} output filter of each inverter to indirectly control its output current. The method can achieve high accuracy in terms of equal current distribution between the power sources. Simulation and experimental results are presented to verify the theoretical analysis.

\textbf{Keywords:} current sharing, UPS, parallel inverters, multi-loop control, active damping

1. Introduction

Parallel UPS systems have attracted considerable attention in the recent years. Paralleling is usually used to improve thermal management, increase the reliability, redundancy, and for size reduction \cite{2}. Although the operation of inverters in parallel has many advantages, there are many challenges that need to be addressed in the system design stage in order to avoid problems that may lead to serious damage to the equipments. Some of these challenges include: equal load current distribution, and minimization of circulating current which results from unequal values of output voltage, frequency, or phase of the inverters \cite{3}, \cite{4}. Due to the above-mentioned challenges, and considering the ubiquity of distributed generation, control algorithms are imperative to ensure proper operation of modular UPS systems. Control schemes can be divided into two main categories, regarding the way of communication: In the first method, the parallel modules are operated without exchange of information. The “droop” method, which is an example of this method, is employed to mimic the performance of parallel generators. However, this method has well-known limitations, such as the inherent existence of trade-off between voltage regulation and current-sharing accuracy \cite{4}. In the second method, intercommunication among the UPS systems exists. Examples of this method include the average load sharing method \cite{5}, the centralized control scheme \cite{6}, and the master-slave control technique \cite{7}. All these methods (and others) are examples of communication-based control.

This paper is based on the second method; namely, communication-based control. Figure 1(a) shows the configuration of one inverter with a \textit{LCL} filter connected at its output. The capacitor voltage is $E_1$ and the load voltage is $V_L$. Normally, inverters operate in current-controlled or voltage-controlled modes, or a combination of both. Current controlled inverters often use \textit{LCL} filters at the output \cite{8}. The output current is controlled in a single loop \cite{8} or double loops with a minor capacitor current or inductor current loop \cite{8}, \cite{9}–\cite{11}, as shown in Fig. 2(a). On the other hand, voltage controlled inverters normally use \textit{LC} filters and control the capacitor voltage directly (Fig. 2(b)), while incorporating a capacitor current or inductor current minor loops \cite{12}, \cite{13}, \cite{14}. The voltage of the capacitor in this case is equal to the load voltage, if the impedance of the feeder is ignored. Applications of voltage-controlled inverters include UPS systems and distributed generation systems in island mode. Current controlled inverters, on the other hand, are used in grid-connected converters,
active filters, and active rectifiers.

As far as parallel UPS systems with LCL filters are concerned, capacitor voltage control is not often discussed in the literature. For parallel UPS systems connected to a load, the circulating current among them can be minimized to zero by controlling the capacitor voltage and phase of all inverters to be equal. Hence, the main contribution of this paper is the proposal of an equal-current distribution control scheme for parallel UPS systems with LCL filters based on controlling the capacitor voltage and phase. The configuration of the proposed capacitor voltage controller for inverters with LCL filters is shown in Fig. 2(c). The main structure consists of a capacitor voltage outer loop and capacitor current inner loop. The output current (I₁) and load voltage (V_L) are indirectly controlled by calculating the reference value of the capacitor voltage and phase continuously based on current feedback signals from other modules. The system is decentralized, which has the advantage that it is independent from a central unit that is vulnerable to failure. Each unit has its own current-sharing control unit to generate a voltage reference.

To highlight the effectiveness of this control scheme, we proceed in this paper as follows: In Section 2 the configuration of the system is demonstrated. Section 3 describes the internal multi-loop control of each unit. Section 4 discusses the generation of the reference capacitor voltage at each unit. Stability analysis is discussed in Section 5. Simulation results and experimental results are presented in Sections 6 and 7, respectively. Finally, Section 8 concludes the paper.

This paper is an extension of a conference paper that has been presented in (2). More analysis and experimental results are presented in this extended version.

2. System Configuration

Figure 1(a) shows the single-phase equivalent representation of one inverter. At the output of the inverter, an LCL filter is connected. Compared to L filters, high-order passive filters provide a more cost-effective solution to PWM switching harmonics. However, the inherent resonance of LCL has the tendency to destabilize the system. A direct way to damp the LCL resonance is to add a passive resistor. This solution is simple for implementation and reliable, but introduces additional power loss into the system. Therefore, in this paper active damping is employed. More details about active damping and multi-loop control are available in Section 3.

L₀ and L₁ are the inverter-side inductor and the load-side inductor, respectively, and C is the capacitance of the filter. The input dc voltage is V_d. This can be obtained using a three-phase ac/dc rectifier at the input or from a separate dc source. u₁ is the PWM output voltage of the inverter, e₁ and i₃ are the capacitor voltage and its current, respectively. i₀ is the inverter-side current, i₁ is the load-side current, and e_L is the load voltage.

Figure 1(b) shows four inverters connected in parallel to a load. The voltage sources represent the capacitors voltages in Fig. 1(a) (e₁, e₂, etc.). The currents i₁, i₂, i₃ are the load-side currents of the inverters. The impedances Z₁, Z₂, Z₃, Z₄ represent the the load-side inductors of the inverters and their equivalent series resistances:

\[ Z_i = R_i + jωL_i \]  \quad (1)

where i = 1, 2, 3, 4, and ω is the angular frequency (ω = 2πf, f = 50 Hz).

3. Internal Control

In this paper, capacitor voltage of LCL-based parallel inverters is controlled in a multi-loop control scheme. The internal control dynamics will be discussed in this section. The two control loops are as follows:

- Capacitor current minor loop, and
- Capacitor voltage outer loop.

Block 1 in Fig. 3(a) shows the block diagram of inverter 1 with multi-loop control. The control is performed in the dq-synchronous frame since a PI controller holds an infinite gain for dc signals, forcing the system to track the dc reference without steady state error. Voltage and current three phase signals are transformed into dc quantities by means of the well-known Park transformation:

\[
\begin{bmatrix}
\varepsilon_a \\
\varepsilon_b \\
\varepsilon_c
\end{bmatrix} = \frac{2}{3} \begin{bmatrix}
1 & -1/2 & -1/2 \\
0 & -\sqrt{3}/2 & \sqrt{3}/2
\end{bmatrix}\begin{bmatrix}
e_d \\
e_q
\end{bmatrix} \quad (2)
\]
Current Distribution between Inverters Using Capacitor Voltage Control

Mohammad Bani Shamseh et al.

Fig. 3. (a) Control scheme composed of block 1: proposed equal-load-sharing control, and block 2: voltage and current control in synchronous frame, (b) block diagram of multi-loop control

\[
\begin{bmatrix}
V_d \\
V_q
\end{bmatrix} =
\begin{bmatrix}
\sin \theta_{\text{ref}} & \cos \theta_{\text{ref}} \\
\cos \theta_{\text{ref}} & -\sin \theta_{\text{ref}}
\end{bmatrix}
\begin{bmatrix}
v_\alpha \\
v_\beta
\end{bmatrix}
\]

where \(\theta_{\text{ref}}\) is the reference phase angle of the grid which can be extracted by means of PLL, as shown in Fig. 3(a).

The block diagram of the closed-loop control of the inverter is shown in Fig. 3(b). The inner loop is the capacitor current loop. The open-loop transfer function of the inner control loop with the capacitor current at the output is:

\[
G_{IC} = \frac{K_p w_m C s (s L_1 + R_1 + R_L)}{s^3 + b s^2 + e s + d}
\]

where \(a = CL_0 L_1\), \(b = L_1 R_0 + L_0 (R_1 + R_L)\), \(e = L_0 + L_1 + R_0 C (R_1 + R_L)\), \(d = R_0 + R_1 + R_L\), \(K_{pum} = V_{dc}/2\), and \(R_L\) is the load resistance.

To analyse the Bode plot of the inner current loop transfer function, the specifications shown in Table 1 will be used. The Bode plot of the open-loop transfer function \(G_{IC}\) is shown in Fig. 4. The Bode diagram of the inner capacitor current exhibits a theoretical gain margin of infinity and a phase margin of \(90^\circ\). The root locus of \(G_{IC}\) is shown in Fig. 5. Notice that all poles are on the left-hand plane and two complex poles move towards the real axis and merge at \(k_c = 0.05\). However, to avoid over compensation in the current loop, and because digital implementation of the system puts limits on the maximum allowable gain to maintain stability of the system due to time delay and Zero Order Hold (ZOH) effect \(^8\), a value of 0.02 for the proportional gain of the inner loop is chosen in this paper.

After designing the capacitor current loop, the next step is to analyse the capacitor voltage loop. The open-loop transfer function of the capacitor voltage loop can be obtained based on the block diagram in Fig 3(b) and the transfer function of the inner current loop in (4) as follows:

\[
G_v = G_{PI} \frac{k_c G_{IC}}{1 + k_c G_{IC}} \frac{1}{C s}
\]

where \(G_{PI}\) is the transfer function of the PI controller:

\[
G_{PI} = k_p + \frac{k_i}{s}
\]

In Fig. 3(b), \(H_T\) is a lead compensator added in the

Table 1. Specifications of one inverter unit

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{dc})</td>
<td>300 V</td>
<td>(R_0)</td>
<td>55.6 mΩ</td>
</tr>
<tr>
<td>(V_L)</td>
<td>100 Vrms</td>
<td>(L_0)</td>
<td>0.6 mH</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>15 kHz</td>
<td>(C)</td>
<td>40 μF</td>
</tr>
<tr>
<td>Output frequency</td>
<td>50 Hz</td>
<td>(R_1)</td>
<td>39 mΩ</td>
</tr>
<tr>
<td>Rated power</td>
<td>5 kVA</td>
<td>(L_1)</td>
<td>1.2 mH</td>
</tr>
</tbody>
</table>
capacitor voltage forward loop. The lead compensator is used to advance the phase of the voltage transfer function in the vicinity of the 0 dB point in order to increase the phase cut-off frequency, resulting in increase in the phase margin of the system. The transfer function of the lead compensator is:

\[ H_T = \frac{1 + \tau_1 s}{1 + \tau_2 s} \]  

where \( \tau_1 > \tau_2 \). In this paper \( \tau_1 = 100 \times 10^{-6} \), \( \tau_2 = 20 \times 10^{-6} \).

The open-loop transfer function of the capacitor voltage loop including the lead compensator is:

\[ G_{vd} = G_v H_T \]  

Figure 6 shows the Bode plots of both \( G_v \) and \( G_{vd} \). Notice that the phase margin of the open-loop transfer function with the lead compensator is significantly larger than that without compensation.

4. Proposed Control Scheme

The proposed current-sharing control method is based on regulating the capacitor voltage of each inverter (\( E_1 \) in Fig. 1(a)). The following steps explain the control scheme of the proposed method. For each inverter, the operation principle of the current-sharing controller (Block 2 in inverter 1 in Fig. 3(a)) is as follows:

1. The output currents of all inverters are measured and the average current is calculated:

\[ I_{ref\,1} = \frac{I_1 + I_2 + \ldots + I_n}{n} = \frac{I_{ref\,1}}{\beta_{ref\,1}} \]  

where \( I_{ref\,1} \) is the reference current calculated at the controller of inverter 1, \( \beta_{ref\,1} \) is the reference current phasor, and \( n \) is the number of parallel inverters.

2. Convert the reference current to the dq-frame:

\[ I_{ref\,1} = I_{ref\,id} + j I_{ref\,iq} \]  

Then, by applying KVL principle, the reference capacitor voltage (\( E_{ref\,1} \)) is calculated as:

\[ E_{ref\,1} = V_{ref\,1}/\beta_{ref\,1} \]

\[ = V_{ref\,1} Z_1 I_{ref\,1} \]

\[ = V_{ref\,1} + (R_1 + j \omega L_1)(I_{ref\,id} + j I_{ref\,iq}) \]  

where: \( E_{ref\,1} \) is the reference capacitor voltage of inverter 1, \( Z_1 \) is the impedance of the output inductor of inverter 1 (\( Z_1 = \frac{|Z_1|}{\beta_{ref\,1}} = R_1 + j \omega L_1 \)), and \( V_{ref\,1} \) is the phase-to-ground reference load voltage (100 V rms in this paper).

The phase of load voltage is synchronised with the grid voltage, which is extracted by the PLL unit in Fig. 3(a), and hence it is considered as the zero reference.

3. Finally, the dq-components of the reference capacitor voltage can be calculated based on (10) as follows:

\[ E_{ref\,id} = V_{ref\,1} + R_1 I_{ref\,id} - j \omega L_1 I_{ref\,iq} \]  

\[ E_{ref\,iq} = R_1 I_{ref\,iq} + j \omega L_1 I_{ref\,id} \]  

The dq components of the reference voltage are used for local multi-loop control at each inverter as discussed in Section 3.

The phasor diagram in Fig. 7 shows the reference load voltage, reference current, and the construction of the reference capacitor voltage for inverter 1 with an inductive load. The reference current is calculated using (9), and has a phase equal to \( \beta_{ref\,1} \). The voltage drop on the load-side inductor is \( (I_{ref\,id} R_1 + j \omega L_1) \). \( E_{ref\,1} \) is then calculated by adding the voltage drop on the inductor with the reference load voltage (\( V_{ref\,1} \)). This process enables indirect control of the output current by regulating the capacitor voltage of the inverter.

It is important to mention that the control scheme uses the parameters \( R_1 \) and \( L_1 \), therefore these values must be known. Moreover, if the impedance of the connecting cables is significant, it should be lumped with the impedance of the output inductor in the controller. Furthermore, in practical systems these values may have some error, and as a result, may cause some error in the load voltage and circulating current between the inverters. However, the circulating current is small in the proposed method. For example, for two parallel UPSs with 5 kVA rated power each, if the inductor of UPS 2 has a 10% error, then, at 10 kVA load, the errors in the load voltage amplitude and phase are 0.14 V and 0.2°, respectively. The circulating current is 1.38% of the load current. The circulating current can be further mitigated by employing the virtual impedance concept to adjust the reference voltage and compensate for the variation in the impedance of the output inductors. More details about the virtual impedance can be found in (7).

For \( n \) parallel inverter, by applying the proposed control algorithm, at steady-state, the system converges to one equilibrium state:
\[ I_1 = I_2 = \ldots = I_n = I_{load}/n \]
\[ E_1 = E_2 = \ldots = E_n = V_{Lref} + Z_1 I_{ref} \]
\[ V_L = V_{Lref} \]

Notice that in the steady state all parallel inverters have equal capacitor voltages. The state guarantees that the circulating current is zero. See equation (A4) in the Appendix for more details.

For inverters with different capacities, the current sharing can be controlled by controlling the ratio of the output inductors. Based on (10), and taking into consideration that the capacitor voltages of all inverters must be equal to eliminate the circulating current, the following equation is obtained:

\[ \frac{I_1}{I_2} = \frac{Z_1}{Z_2} \]  

(14)

5. Analysis of Complete System Stability

The time average model of a system of two parallel inverters in synchronous DQ reference frame is:

\[
\begin{bmatrix}
\frac{d}{dt} I_{id} \\
\frac{d}{dt} I_{iq}
\end{bmatrix} = \begin{bmatrix}
\frac{1}{L_0} \left[U_{id} - E_{id}\right] + \frac{-R_0/L_0}{\omega} [\omega] I_{id} \\
\frac{1}{L_1} \left[U_{iq} - E_{iq}\right] + \frac{-R_1/L_1}{\omega} [\omega] I_{iq}
\end{bmatrix}
\]

\[
\begin{bmatrix}
\frac{d}{dt} E_{id} \\
\frac{d}{dt} E_{iq}
\end{bmatrix} = \begin{bmatrix}
\frac{1}{C} \left[I_{id} - I_{id}\right] + \frac{0}{\omega} [\omega] E_{id} \\
\frac{1}{C} \left[I_{iq} - I_{iq}\right] + \frac{0}{\omega} [\omega] E_{iq}
\end{bmatrix}
\]

\[
\begin{bmatrix}
\frac{d}{dt} I_{d} \\
\frac{d}{dt} I_{q}
\end{bmatrix} = \begin{bmatrix}
\frac{1}{L_1} \left[E_{id} - V_{id}\right] + \frac{-R_1/L_1}{\omega} [\omega] I_{d} \\
\frac{1}{L_1} \left[E_{iq} - V_{iq}\right] + \frac{-R_1/L_1}{\omega} [\omega] I_{q}
\end{bmatrix}
\]

\[
\]

(15)

where \( i = 1, 2 \) denotes the index of the inverter, \( L_0 \) and \( R_0 \) are the inverter-side inductance and resistance, \( C_1 \) and \( R_1 \) are the output-side inductance and resistance, and \( C \) is the capacitance. For simplicity, the two inverters have the same \( LCL \) filters parameters. Other current and voltage variables are as shown in Fig. (1a). The PWM output voltage of inverter \( i \) in the synchronous frame, \( U_{idq} \), is represented as:

\[ U_{idq} = K_{pwm} \left[k_i k_p e_{idq} + k_i \int e_{idq} + C \frac{de_{idq}}{dt} \right] \]  

(16)

where \( e_{idq} \) is the voltage error signal (\( e_{idq} = E_{ref/dq} - E_{idq} \), \( e_{2dq} = E_{ref/2dq} - E_{2dq} \)), \( E_{ref/dq} \) is as shown in (11).

A complete state space model of two parallel inverters operating under the proposed scheme can now be derived based on the time average model around the equilibrium point. Using (11), (15), and (16), and applying small signal perturbations, the state space model in matrix form can be described as:

\[ \Delta X = A \Delta X + \frac{1}{L_0} \Delta U \]  

(17)

where \( \Delta X \) is the state vector, \( \Delta X = [\Delta i_{0id} \Delta i_{0iq} \Delta E_{id} \Delta E_{iq} \Delta i_{1d} \Delta i_{1q} \int \Delta e_{idq} \Delta e_{iq} \Delta i_{0dq} \Delta i_{2dq} \Delta E_{2dq} \Delta E_{2dq} \Delta i_{2d} \Delta i_{2q} \int \Delta e_{2dq} \Delta e_{2dq} ]^T \), \( \Delta U \) is the system input, \( \Delta U = [\Delta U_{id} \Delta U_{iq} \Delta U_{jdq} \Delta U_{jdq} ]^T \). \( A \) is the state matrix.

The system input, \( \Delta U \), can be represented in terms of the state variables. Based on (11), (15), and (16), the system input is represented as:

\[ \Delta U = B \Delta X \]  

(18)

Matrices A and B are shown in (A1) and (A2) in the Appendix.

The closed-loop system can now be represented as:

\[ \Delta X = (A + B) \Delta X \]  

(19)

The stability of the system can be investigated by calculating the eigenvalues of (19). Figure 8(a) shows the poles of the system for \( k_c = 0.02, k_p = 50, k_i = 2000 \). All poles are in the left hand plane, which proves that the system is stable. To investigate the effect of the gains in the inner current loop and outer voltage loop on the stability of the system, the low-frequency poles will be considered since they are close to the imaginary axis. Figure 8(b) shows the dominant poles of the system (marked with a circle in Fig. 8(a)). Increasing the gain of the current loop \( k_c \) moves the poles to the left, resulting in faster response. Increasing the proportional gain of the voltage loop \( k_p \), on the other hand, moves the eigenvalues to the right, which means that excessive gain in the voltage loop results in slow dynamic response and reduces the stability margin of the system.

6. Simulations

Two 173-Vrms/5 kVA 50 Hz inverters are connected in parallel. The two units have the same parameters as shown in Table 1. The robustness of the control algorithm against load variation and disconnection of inverters from the network will be discussed in this section using simulation. In all simulation results, the proposed control is activated at \( t = \ldots \)
Current Distribution between Inverters Using Capacitor Voltage Control

Mohammad Bani Shamseh et al.

Fig. 9. Circulating current between two parallel inverters for different values of $L_1$

6.1 Case I: Resistive Load
A 6 kW load is connected at the output of the parallel inverters. First, the circulating current between the inverters for different values of load-side inductor ($L_1$) are shown in Fig. 9. Notice that even for a small inductance, the controller suppresses the circulating current to zero in the steady state. Figure 10(a) shows the output currents of the two inverters ($I_1$ and $I_2$). Notice that at the beginning, the two currents are identical and have the same amplitude. At $t = 0.4$ s, the load is decreased to 4 kW. The system maintains a proper current distribution even under load variation. Finally, at $t = 0.7$ s, unit 2 is disconnected from the system. Unit 1 detects the fault in unit 2 and adjusts the control law of its load-sharing controller. Since now only unit 1 is operating, the average current in (9) equals to the output current of inverter 1 ($I_1$). After adjustment of the control law, the whole load current is now supplied by this unit.

Figure 10(b) shows the load voltage throughout the whole process. Notice that the control scheme guarantees a constant, uninterrupted load voltage even in the case of failure of one unit.

Figure 10(c) shows the capacitor voltage amplitude and phase of the two inverters, calculated from the direct and quadrature components. The two units have equal capacitor voltages, which means the circulating current is zero. At the instant the load is decreased, controllers of each UPS detect the decrease in the output currents and adjust the reference capacitor voltage based on (11). As shown in Fig. 10(c), the amplitude and phase angle decrease to meet the new load requirement. When inverter 2 is disconnected at $t = 0.7$ s, $I_2$ inverter 1 adjusts its reference capacitor voltage in accordance with (9) and (11), leading to an increase in the magnitude and phase angle of the capacitor voltage.

6.2 Case II: Reactive Load
The same structure of the inverters in case I is used to supply power to a 6 kVA load with power factor of 0.9, and the results are shown in Fig. 11. First, the output currents and their respective phase angles are shown in Fig. 11(a). The output currents are equal in the steady state. Moreover, their phase angles are shifted by $-25.8$ deg from the zero reference, which corresponds to a 0.9 lagging power factor.

The circulating current between the inverters is shown in Fig. 11(b). In the steady state the control scheme suppresses the circulating current to zero. Finally, the load rms voltage and phase are shown in Fig. 11(c).

6.3 Case III: Grid Failure Condition
The synchronization between the parallel UPS modules in the normal operation mode is performed by means of a PLL which takes its input from the voltage grid. However, in case of grid failure or voltage distortion conditions, the output of the PLL might be distorted and therefore an alternative source of synchronization should be available.

The load voltage bus is accessible to all modules and can be used to generated the reference phase in case of grid failure. As shown in Fig. 12, the input to the PLL becomes the three phase load voltage. Notice that in normal conditions, the load voltage is in phase with the grid voltage, and when the PLL
detects distortion in the grid voltage, it switches to the load voltage and the system is disconnected from the grid. Figure 13 shows the results for the grid failure condition. Three inverters are connected to a 6 kVA load with 0.9 power factor. At $t = 0.305$ s a fault occurs at the grid which causes the PLL to switch its input to the load voltage. Figure 13(a) shows the currents and their phase angles. Notice that the system continues its operation without interruption and the system maintains stability. Figure 13(b) shows the single phase grid voltage and load voltage. The load voltage is synchronized with the grid and at the steady state it becomes equal to the grid voltage. When the fault occurs, the grid is disconnected without interruption in the load voltage. At $t = 0.45$ s an additional 2 kW resistive load is connected in parallel. The equal current distribution is maintained.

### 7. Experiments

Two inverters each with a 5 kVA rated power are connected in parallel. The three phase grid voltage is used as the input to the inverters. Each inverter has a built-in rectifier which generates 300 V dc, which is used as the input for the inverters. The control is based on TMSF28335 DSP. The load is 1 kw and the specifications of each inverter are as shown in Table 2.

Figure 14 shows the capacitor voltage of unit 1 ($E_1$), as well as its capacitor current ($I_{C1}$). Figure 14 also shows the dq-components of the reference capacitor voltage for the same unit. The reference dq-components of the capacitor
Current Distribution between Inverters Using Capacitor Voltage Control

Mohammad Bani Shamseh et al.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{dc}$</td>
<td>300 V</td>
<td>three-phase ac/dc rectifier</td>
</tr>
<tr>
<td>$f_s$</td>
<td>15 kHz</td>
<td>sampling frequency</td>
</tr>
<tr>
<td>$D_T$</td>
<td>5 μs</td>
<td>dead time</td>
</tr>
<tr>
<td>$L_0$</td>
<td>0.6 mH ± 10%</td>
<td>dust core</td>
</tr>
<tr>
<td>$R_0$</td>
<td>55.6 mΩ</td>
<td>equivalent series resistance</td>
</tr>
<tr>
<td>$C$</td>
<td>40 μF ± 6%</td>
<td>polypropylene capacitor</td>
</tr>
<tr>
<td>$L_1$</td>
<td>1.2 mH ± 10%</td>
<td>silicon steel core</td>
</tr>
<tr>
<td>$R_1$</td>
<td>39.6 mΩ</td>
<td>equivalent series resistance</td>
</tr>
<tr>
<td>$P_0$</td>
<td>5 kVA</td>
<td>rated power</td>
</tr>
</tbody>
</table>

8. Conclusion

This paper has presented a new method to control parallel UPS modules based on capacitor voltage control of $LCL$ filters. The output current of each inverter is indirectly controlled by regulating its capacitor voltage. As opposed to centralized control and Master-Slave control, there is no central unit, nor a master unit. Each unit has a current-sharing controller which is used to calculate the reference capacitor voltage for this unit. The main advantages of the proposed method include:

- Flexibility to add new units or disconnect operating units without system interruption.
- Precise equal load distribution with zero circulating current.
- Robustness against load variation and excellent transient response.
- Easy to implement.
- Ability to maintain synchronization even in case of grid failure without interruption.

References


(8) J. wang, J.D. Yan, L. Jiang, and J. Zou: “Delay-Dependent Stability of Single-Loop Controlled Grid-Connected Inverters with LCL Filters”, IEEE
The matrices in equation (19) are shown in (A1) and (A2): 

\[
A = \begin{bmatrix} A_{ii} & A_{ij} \\ A_{ji} & A_{jj} \end{bmatrix}, \quad A_{ii} = \begin{bmatrix} -\frac{B_i}{L_0} & \omega & \frac{1}{L_0} & 0 & -\frac{B_i}{L_0} & 0 & 0 & 0 & 0 \\ -\omega & -\frac{B_i}{L_0} & 0 & \frac{1}{L_0} & 0 & 0 & 0 & 0 & 0 \\ \omega & 0 & 0 & 0 & -\frac{B_i}{L_0} & 0 & 0 & 0 & 0 \\ -\omega & 0 & 0 & 0 & -\frac{B_i}{L_0} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{B_i}{L_0} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{B_i}{L_0} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, \quad A_{jj} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} 
\]

\[
B = \begin{bmatrix} B_1 \\ B_2 \\ B_3 \\ B_4 \end{bmatrix}, \quad B = \begin{bmatrix} B_1 & B_2 & B_3 & B_4 \end{bmatrix}^T = \begin{bmatrix} -k_c & 0 & -k_c & 0 & k_c(1 + \frac{R_c}{L_1} - \frac{\omega^2L_1C_k}{2}) & 0 & k_c(k_cR_1 + \omega C_kR_1) \\ 0 & -k_c & 0 & -k_c & 0 & k_c(k_cR_1 + \omega C_kR_1) & 0 & k_c(k_cR_1 + \omega C_kR_1) \\ 0 & 0 & 0 & 0 & 0 & \frac{k_c}{L_1}(k_cR_1 + \omega C_kR_1) & 0 & 0 \end{bmatrix}.
\]

\[I_1 = \frac{E_i}{Z + \frac{k_c}{L_1} + \frac{\omega L_1 C_k}{2}} \frac{k_c(1 + \frac{R_c}{L_1} - \frac{\omega^2L_1C_k}{2})}{Z(L + \frac{k_c}{L_1} + \frac{\omega L_1 C_k}{2})} [E_2 + \ldots + E_n]. \]

\[I_i = \frac{E_i}{Z + nZ_L} \frac{Z_L}{Z(L + nZ_L)} [E_1 - \sum_{j=1}^{n} E_j]. \]

Similarly, equations of output currents of all other units can be derived in the same manner as in (A3).

Equation (A3) can be simplified and written in a more general form. For \( n \) parallel inverters with output voltages \( E_1, E_2, \ldots, E_n \), output impedance equals to \( Z \), and a load impedance of \( Z_L \), the output current of unit \( i \) is:

\[I_i = \frac{E_i}{Z + nZ_L} \frac{Z_L}{Z(L + nZ_L)} [E_1 - \sum_{j=1}^{n} E_j]. \]
Mohammad Bani Shamseh (Non-member) received the B.S. degree in electrical engineering from An Najah National University in Palestine in 2011, the M.S. in electrical engineering in 2014 from Yokohama National University, Japan, where he is currently working toward the Ph.D. degree in electrical engineering. His current research interests include uninterruptible power supplies, distributed generation systems, and control of power converters.

Teruo Yoshino (Fellow) received M.E. degree in electrical engineering from Yokohama National University, Kanagawa, Japan and joined Toshiba in 1978. He has been working for developments on power electronics products for high voltage and high power applications including HVDC and SVC. In 2003, he earned Ph.D. at Yokohama National University. He moved to Toshiba Mitsubishi Electric Industrial Systems Corporation, established also in 2003. There, he works as a senior fellow engineer of power electronics. He is a Fellow of IEE of Japan.

Atsuo Kawamura (Fellow) received the Ph.D. degree in electrical engineering from the University of Tokyo in 1981. After the five-year-stay at the University of Missouri-Columbia as a faculty member, he joined the department of electrical and computer engineering at Yokohama National University in 1986, and now he is a professor. His interests are in the fields of power electronics, digital control, electric vehicles, train traction control and robotics. He received Transaction Paper Award from IEEE in 1988, 2001 and 2002, also from IEE of Japan in 1996. Dr. Kawamura is an IEEE Fellow, and Fellow of the IEE of Japan.