Multilevel Inverter Topology Using Current Path Change for Zero Current Switching

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In motor drive applications, a high switching frequency is required to mitigate current harmonics, which cause a copper loss. However, the high switching frequency makes the switching loss large. Hence, some switching loss reduction techniques have been studied in the past. These techniques have some problems. This paper proposes a multilevel inverter topology for switching loss reduction. Because of provision of multiple current paths, the proposed inverter realizes the zero current switching. Consequently, a loss of the whole system including an inverter and motor can be reduced with a higher switching frequency. The switching loss of the proposed inverter is smaller than that of the conventional one. It was verified that the proposed inverter has some advantages at high switching frequency, through calculations.

Keywords: multilevel inverter, switching loss, bidirectional switch, topology, zero current switching

1. Introduction

In motor drive applications, mitigating current harmonics is very important. The current harmonics cause a torque ripple and copper loss. Therefore, multilevel inverters are better than two level inverters. Multilevel inverters can reduce voltage stress across semiconductor switches which connect other switches in series. Thus, multilevel inverters have other advantages such as reducing dv/dt , voltage total harmonic distortion and electromagnetic interference. These characteristics are suitable for motor drive applications.

In general terms, multilevel inverters are categorized into three types by their topologies; Neutral Point Clamped (NPC), Flying Capacitor (FC) and Cascaded H-Bridge (CHB). The NPC inverters are used for high power AC motor drive applications, which have been studied to increase efficiency of trains⁽¹⁾⁽²⁾. However, they have a disadvantage of the charge imbalance of capacitors, which need complicated modulation methods or extra circuits⁽³⁾⁽⁴⁾. The CHB inverters are used for very high power applications which demand power quality; static var compensator and distributed generations using renewable energy⁽¹⁾⁽⁵⁾. However, they require multiple isolated DC voltage sources⁽⁶⁾. By using fuel cells and photovoltaic cells, the problem can be overcome⁽⁷⁾. The FC inverters are used for high bandwidth high switching frequency applications⁽¹⁾. However, they require numerous capacitors. As the number of voltage levels increase, the large number of capacitors and the complex voltage balancing methods are required⁽⁶⁾. Additionally, a generalized

Table 1. Comparison between multilevel inverters

	P2	FC	NPC	Proposed
Voltage stress of switches	$\frac{1}{N-1}$	$\frac{1}{N-1}$	$\frac{1}{N-1}$	$\frac{4}{N+1}$ or $\frac{8}{N+1}$
Number of switches	$(N-1)N$	$2(N-1)$	$\frac{2(N-1)}{\text{Diode: } 2(N-2)}$	$2(4N-13)$
Number of capacitors	$\frac{1}{2}(N-1)N$	$N-2$	$N-1$	$\frac{1}{2}(N-1)$
Voltage self balancing	itself	×	×	itself
Voltage stress of capacitors	$\frac{1}{N-1}$	$\frac{1}{N-1} \cdot \frac{N-2}{N-1}$	$\frac{1}{N-1}$	$\frac{1}{N-2}$

multilevel (P2) inverter topology was proposed⁽⁸⁾. FC inverters and NPC inverters can be derived from that inverter which can lead some new structure. Although the generalized multilevel inverter can balance the capacitor voltage, it requires numerous capacitors and switches.

In addition, a higher switching frequency is required in PWM drive in order to mitigate a copper loss. However, the higher switching frequency increases a switching loss of inverters⁽⁹⁾. Therefore, techniques to reduce the switching loss have been studied. The soft switching technology has been used to reduce the switching loss. It uses a LC resonance to keep a voltage or current of a switch zero during the entire turn-on and turn-off transition. Nevertheless, it has some limitations; a limited drive range, increase of conduction loss, and more complicated circuit⁽¹⁰⁾⁽¹¹⁾.

The proposed topology has some advantages to the conventional topologies, which are described in Table 1. Although the voltage stress of switches to DC link voltage and the number of switches are larger than those of conventional topologies, the proposed topology can naturally balance capacitor voltage. Moreover, it does not need extra circuits for the zero current switching. This paper proposes a multilevel inverter topology using current path change for the zero current switching to reduce the switching loss. When the output voltage changes, the current path and the switch condition

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change at different timing by using multiple current paths, which realizes zero current switching.

This paper is organized as follows. In section 2, the principle of proposed inverter is presented. In section 3, the power loss is compared with the FC inverter by calculation. CHB inverters do not work with single DC voltage source and NPC inverters have a lot of diodes which cause large switching loss. For these reasons, these topologies are excepted in the comparison. Finally, the conclusions are presented in section 4.

2. Proposed Topology

2.1 General Topology Figure 1 illustrates the proposed inverter topology, where n is the number of capacitors of the upper side or the lower side. All the capacitors are charged at the half of DC source voltage V_{dc} without extra circuits to balance the capacitor voltage. It has a charge-pump structure. The number of capacitors connecting to DC source voltage in series changes the output voltage which has $2n + 1$ steps. Its output voltage has $2n + 1$ steps. Assuming that the DC source is constant, the larger number of output voltage steps, the larger voltage the inverter can output. When the output voltage is changed to different level, the order of switching must be considered to prevent from short-circuit. The voltage across each capacitor is $V_{dc}/2$ and the voltage across each switch is $V_{dc}/2$ or V_{dc} .

2.2 Current Path of Seven Level Inverter The most basic proposed inverter is five level topology. However, considering the higher level extension, the proposed seven level topology which is illustrated in Fig. 2 is suitable. Hereinafter, seven level topology is discussed. Figure 3 illustrates the switch combinations on each voltage level V_{out} . Behavior of capacitors of seven level topology is described by the following.

- For voltage level 0 V, all capacitors are connecting to DC source in parallel and charged at $1/2 V_{dc}$. Figure 2(a) illustrates this conduction path. Voltage stresses of $S_1, S_2, S_5, S_6, S_{10}$, and S_{11} are $1/2 V_{dc}$.
- For voltage level $1/2 V_{dc}$, all capacitors are connecting to DC source in parallel and charged at $1/2 V_{dc}$. Figures 2(b), (c) illustrate these conduction paths. Voltage stresses of S_1, S_2, S_5 , and S_6 are $1/2 V_{dc}$. Those of S_{10} or S_{11} are V_{dc} .
- For voltage level V_{dc} , C_{11} and C_{21} are charged. C_{12} is discharging. Figure 2(d) illustrates this conduction path. Voltage stresses of S_1, S_2, S_7, S_8 , and S_9 are $1/2 V_{dc}$. Those of S_6 and S_{11} are V_{dc} .
- For voltage level $3/2 V_{dc}$, C_{11} and C_{12} are discharging. Figure 2(f) illustrates this conduction path. Voltage stresses of S_3, S_4, S_7, S_8 , and S_9 are $1/2 V_{dc}$. Those of S_2, S_6 , and S_{11} are V_{dc} .

Capacitors symmetrically work up side down in the cases that output voltage is negative. Theoretically, switches are classified to two groups by these maximum voltage stresses. The classification is discussed in section 3.

2.3 Principle of Zero Current Switching Realized by Current Path Change How to realize the zero current switching is explained. When the output voltage of the proposed topology changes, four MOSFETs relate the change of the current path. The order of switching is determined in

Fig. 1. Proposed topology phase-leg

Fig. 2. Proposed single-phase seven level topology

Fig. 3. Current paths patterns of output voltage

Fig. 4. Bidirectional switch

order to prevent capacitors from short circuit and keep the current continuous. Hence, switches must be bidirectional switches which can control a current direction consists of two MOSFETs illustrated in Fig. 4. S_{AB} consist of two MOSFETs, S_A and S_B which are used for the following explanation. S_{CD} is the same manner to S_{AB} . In Fig. 4, a left MOSFET can control the current flowing to the right and a right MOSFET can control the current flowing to the left. In the seven level inverter, switches are classified as illustrated in Table 2. The order of switching is classified to four cases by the current direction and the voltage change. Except for S_8 ,

Table 2. Switch classification

Change of output voltage	S_{AB}	S_{CD}
$\frac{1}{2}V_{dc} \leftrightarrow V_{dc}$	S_3	S_1
$V_{dc} \leftrightarrow \frac{1}{2}V_{dc}$	S_7	S_5
$\frac{1}{2}V_{dc} \leftrightarrow 0$	S_8	S_{10}
$0 \leftrightarrow -\frac{1}{2}V_{dc}$	S_8	S_{11}
$-\frac{1}{2}V_{dc} \leftrightarrow -V_{dc}$	S_9	S_6
$-V_{dc} \leftrightarrow -\frac{1}{2}V_{dc}$	S_4	S_2

Fig. 5. Current path change when current is positive and voltage gets larger

Fig. 6. Current path change when current is negative and voltage gets larger

the cases when the output voltage get larger is explained as follows. In other cases, switches work in reverse order.

Figure 5 illustrates a case that the current is positive and the voltage gets larger. Firstly, S_A turns off and S_D turns on simultaneously. The current through S_A keeps flowing, which does not cause the turn-off loss. The current is not flowing through S_D , which does not cause the turn-on loss. Secondly, S_C turns on. Then, a body diode of S_A turns off and the current path changes from one passing through S_A and S_B to one passing through S_C and S_D . That turn-off causes a reverse recovery loss. Finally, S_B turns off, which does not cause the turn-off loss as the current is not flowing through S_B .

Figure 6 illustrates a case that the current is negative and the voltage gets larger. Firstly, S_D turns on. The current is

Fig. 7. Current path change when current is positive and voltage gets larger in the case including S_8 Fig. 8. Current path change when current is negative and voltage gets larger in the case including S_8

not flowing through S_D , which does not cause the turn-on loss. Secondly, S_A turns off and the current path changes from one passing through S_A and S_B to one passing through S_C and S_D . Finally, S_B turns off and S_C turns on simultaneously. The current is not flowing through S_B , which does not cause the turn-off loss. The current of S_C keeps flowing, which does not cause the turn-off loss.

The relation between the generalized explanation and the actual switches (S_1 - S_{12}) behavior is illustrated in Table 2. The cases including S_8 is shown in Figs. 7, 8. Although the positional relation of S_A , S_B , S_C , and S_D is different from the former, switches similarly work. Although the current direction is opposite to top leg, the bottom leg works similarly, whose switches are classified in Fig. 9. In all cases, S_B and S_D realize the zero current switching. Although the reverse recovery loss is caused, a sum of these losses are reduced.

The actual output voltage and current are illustrated in Fig. 10. Supposed a motor, the load is only an inductance.

The encircled part in Fig. 10(a) is focused on, in order to demonstrate realizing the zero current switching. The

Fig. 9. Switch classification of bottom phase leg

Fig. 10. Output voltage and current

Fig. 11. Waveforms of S_B and S_D

waveforms relating to the switches, S_B and S_D (S_1 and S_3) are illustrated in Fig. 11. The output voltage gets larger and the output current is positive. This case corresponds to the switching pattern in Fig. 11(a). When the gate signal of S_B changes to low in Fig. 11(a), the current through S_B is zero in Fig. 11(c), which does not cause the switching loss. When the gate signal of S_D changes to high in Fig. 11(a), the current

Fig. 12. Waveforms of S_A and S_C Fig. 13. Capacitor C_{11} voltage

through S_D is zero in Fig. 11(c), which does not cause the switching loss. These results confirm that the zero current switching is realized in S_B and S_D . The gate signal of S_4 in Fig. 2 is illustrated in Fig. 11(a). As illustrated in Fig. 3, S_4 turns off when the output voltage is changed from V_{dc} to $\frac{3}{2}V_{dc}$. In the switching pattern explanation using Fig. 5, the S_4 effect is not referred for simplification. Turning off S_4 makes C_{11} and C_{21} floating. Because of this effect, the current through C_{11} and C_{21} become zero, which changes the current through S_B as illustrated in Fig. 11(c).

Figure 12 illustrates waveforms of S_A and S_C . After the gate signal in Fig. 12(a) become low, the voltage across S_A gets larger in Fig. 12(b) and the current through S_A get smaller in Fig. 12(c) simultaneously. This is a cause of the reverse recovery loss of S_A .

Figure 13 illustrates the voltage of C_{11} . All the capacitors have already been charged. Compared with the voltage immediately after start, the voltage oscillation after ten second is small. Therefore, the proposed inverter can balance the capacitor voltage.

3. Loss Analysis

This section analyzed losses. The analysis verified that the proposed topology has a high efficiency. The loss of MOSFETs is classified to a conduction loss and a switching loss. The conduction loss is caused by on-resistance of the MOSFET. On the other hand, the switching loss is caused when

Table 3. Analysis conditions

Output voltage V_0	100 Vrms
Output current I_0	1 Arms
Output voltage frequency f	60 Hz
Current phase lag	$\frac{\pi}{3}$
Proposed (group1)	2SK3176
Proposed (group2)	2SK1381
FC	2SK2233

the MOSFET turns on or off. In addition, a reverse recovery loss is included in switching loss in this paper.

Firstly, the conduction loss is described as

$$P_{\text{con}} = R_{\text{DS(on)}} I_D^2, \dots \dots \dots (1)$$

where $R_{\text{DS(on)}}$ and I_D are respectively on-resistance of MOSFET and drain current.

Secondly, the switching loss is a summation of turn-on loss and turn-off loss. The switching loss of the proposed inverter $P_{\text{sw-p}}$ is described as

$$P_{\text{sw-p}} = f_s \sum_{k=0}^{\lfloor \frac{f_c}{f} \rfloor} (E_{\text{on-p}} + E_{\text{off-p}} + E_d), \dots \dots \dots (2)$$

where f_s , $E_{\text{on-p}}$, and $E_{\text{off-p}}$ are respectively switching frequency, the turn-on loss, and the turn-off loss of the proposed inverter. On the other hand, the switching loss of the FC inverter $P_{\text{sw-f}}$ is described as

$$P_{\text{sw-f}} = 12f_s \sum_{k=0}^{\lfloor \frac{f_c}{f} \rfloor} (E_{\text{on-f}} + E_{\text{off-f}}), \dots \dots \dots (3)$$

where $E_{\text{on-f}}$ and $E_{\text{off-f}}$ are respectively the turn-on loss and the turn-off loss of the FC inverter. There is a difference of the drain-source voltage between the proposed inverter and the FC inverter, which affects the on-resistance. The on-resistance of the proposed inverter is larger than that of the FC inverter. However, the number of turn-on or off times is reduced by using the proposed inverter and some switches realize the zero current switching.

In case of the seven level inverter, parameters are listed in Table 3. It is assumed that the capacitances are large enough to keep the capacitor voltage constant. Considering the output current and voltage, MOSFETs are selected. In Table 3, MOSFETs of the proposed inverter is classified with their maximum drain-source voltage. That voltage of the group2 is half as much as that voltage of the group1. The group1 includes S_C and S_D . On the other hand, the group2 includes S_A and S_B . The following calculations are based on a reference⁽¹²⁾.

Figure 14 illustrates the conduction loss under the condition of Table 3 except for the output current. The result is calculated from Eq. (1). In Fig. 14, the conduction loss of the proposed inverter is larger than that of the FC inverter. However, the difference is small.

The switching loss of the proposed inverter decreases by 63.3% compared with the FC inverter in Fig. 15. This comparison is calculated from Eqs. (2) and (3) under the conditions of Table 3. This result confirms that the proposed topology reduces the switching loss by realizing the zero current switching.

Fig. 14. Comparison of conduction loss

Fig. 15. Comparison of switching loss

Fig. 16. Comparison of total loss

Figure 16 illustrates a total loss including the conduction loss and switching loss under the conditions of Table 3 except the output current which is calculated from Eqs. (1)–(3). Its hatched area illustrates that the total loss of the proposed inverter is smaller than that of the FC inverter. It indicates that the proposed topology is suitable for the high switching frequency PWM drive.

4. Conclusions

This paper proposes a multilevel inverter topology for a switching loss reduction. The proposed topology has some advantages to the conventional multilevel inverter topologies. The proposed topology does not require multiple DC sources, extra circuits to balance the capacitor voltage, and a lot of capacitors. Especially, the proposed topology itself realizes the zero current switching without extra circuits. The loss of the proposed inverter and the FC inverter are analytically compared. Consequently, compared with the FC inverter, the switching loss of the proposed inverter was reduced by 63.3%. It was verified that the proposed inverter can reduce the switching loss and it has an advantage at high switching frequency. The switching loss reduction enables the switching frequency to be higher, which reduces the copper loss.

As a result, the proposed contributes to a total loss reduction including the inverter and motor. In order to realize the usefulness, this paper proposed the original topology for the zero current switching without LC resonance.

Future work includes to reduce capacitance and to improve a limited switching frequency. Owing to the proposed topology which uses a charge pump structure, the capacitors charge and discharge repetitively with the output voltage frequency or the switching frequency. Hence, the proposed topology needs large capacitances. In addition, some steps are required when the conduction path changes, which makes the transition longer. In order to solve these problems, in the future, the switching pattern will be improved to reduce the number of steps.

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