A Method of Junction Temperature Estimation for SiC Power MOSFETs via Turn-on Saturation Current Measurement

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Maintaining the operating junction temperature of a SiC Power MOSFET within a safe and tolerable range is crucial not only for safety reasons, but also for reliable operation, as thermal transient is one of the major stressors that threaten a device’s life span. Conventional methods use thermal sensors for temperature monitoring. However, these sensors require extra space, and the measurement accuracy is affected by their position. Besides, they are unable to track the transient temperature variation owing to relatively slow response time. This paper proposes a new temperature sensor-less method to estimate the junction temperature of SiC power MOSFETs by measuring the device’s turn-on saturation current ($I_{D,sat}$). The device’s square root of the saturation current ($\sqrt{I_{D,sat}}$) and threshold voltage ($V_{th}$) can be extracted and adopted as junction temperature estimators. Compared to the threshold voltage, the square root of the saturation current has the advantage of a shorter test time. The feasibility of this temperature estimation method has been experimentally verified. The results suggest that the proposed method can be used as an alternative for effective online junction temperature monitoring.

Keywords: junction temperature estimation, saturation current, SiC Power MOSFET, threshold voltage

1. Introduction

Growing electrical power demand from various application sectors has driven the design trend of power electronic converters toward higher power density. A high power density design achieves less conduction loss per unit area, higher integration freedom, and hence, lowers the installation cost. Owing to the excellent material property for high temperature and fast switching operation, silicon carbide (SiC) power MOSFET has the full potential to become the key player of next generation high power density converters (HPDCs). Unfortunately, HPDCs are failure-prone, as they are continuously stressed by electrical and thermal strains. Any unexpected failure can lead to unnecessary maintenance cost and even worse, safety hazards. As the backbone and one of the most fragile element in a HPDC, it is crucial to identify early signs of abnormalities of SiC power MOSFETs before they develop into catastrophic failures, which necessitates the need for electronic health monitoring (EHM) technology.

Monitoring the junction temperature during the operation of a SiC MOSFET is essential since thermal stress is closely correlated to device wear-out. Direct measurement of device temperature requires sensors integrated on the chip or being part of it. However, such sensors occupy the chip’s active area and compromise the device’s current carrying capability.

Power module manufacturers often incorporate temperature sensors near to the die for junction temperature measurement, such as negative temperature coefficient (NTC) thermistor, where the measurement accuracy depends greatly on sensor placement. Such thermal sensors exhibit relatively slow response time that affect the capability of transient temperature measurement in real-time.

Electrothermal model∗∗ is an alternative that have been widely used in industrial applications. Junction temperature can be estimated based on the loss and thermal data given in semiconductor datasheet. Today, several semiconductor manufacturers have provided software tools for junction temperature simulation, such as Infineon’s IPOSIM∗∗, Semikron’s SemiSel∗∗ and Mitsubishi’s MELCOSIM∗∗. As the data available in datasheet are generic, where the worst case is often considered, the junction temperature is tend to be overestimated. Although more accurate thermal model can be characterized at laboratory condition, it is difficult to have precise power loss measurement especially under operating condition. Also, a pre-characterized thermal model is not valid throughout the life span of a power device as device aging affects the package’s thermal path integrity.

There are a great number of studies dedicated on utilizing measurable temperature-sensitive electrical parameters (TSEPs) for junction temperature estimation. On-state resistance is a widely accepted static TSEP for power MOSFET∗∗. However, its validity is influenced by package-related deteriorations, which is the most commonly observed failure in real applications. Instead, past studies had put efforts on threshold voltage ($V_{th}$) measurement by capturing gate-to-source voltage ($V_{GS}$) when the device current is zero during turn-on transition∗∗−∗∗, for its load independent nature and is

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unaffected by package-related deteriorations. This method, however, requires high-speed measurement circuits. Otherwise, the switching time has to be extended with large external gate resistor. There are also methods adopting dynamic TSEPs during switching transition, such as gate turn-on, turn-off delay, device current and voltage switching rate\(^{(9)-(12)}\). These TSEPs, however, are easily affected by interconnection conditions and are susceptible to noise. Besides, the required sensing resolution typically ranges from nanosecond to picosecond, which requires current sensor with very large bandwidth, and is more stringent for SiC MOSFET, as it is less temperature sensitive compared to silicon (Si) devices\(^{(13)}\). Moreover, low temperature sensitivity implies that any slight measurement error can lead to misleading information.

To address the measurement difficulties of existing methods, a new sensor-less solution to mitigate the measurement error and the measurement circuits’ bandwidth requirement is proposed. This paper extends the results in\(^{(14)}\) with further demonstration of the online junction temperature monitoring feasibility on a boost converter. The results suggest a possible potential role of the proposed method in the development of future EHM system. The rest of the paper is organized as follows. Section 2 describes the details of the proposed method. The concept is experimentally validated in Section 3. Section 4 demonstrates the online temperature monitoring potential of the proposed method on a boost converter. Section 5 concludes this paper.

2. The Proposed Method

2.1 Principle During the switch-on transition of a SiC power MOSFET, it always experiences the saturation region before it exhibits the resistive behavior when it is fully turned on. Figure 1 illustrates the four phases (phase A to D) during the turn-on transition of a SiC power MOSFET with gate-to-source voltage \(V_{GS}(t)\), device current \(I_{D}(t)\) and drain-to-source voltage \(V_{DS}(t)\) shown. The saturation region is defined by \(V_{th} < V_{GS}(t) < [V_{GS} + V_{th}]\) as marked by the shaded area, which incorporates phase B and parts of phase C (Miller plateau period). Since the SiC power MOSFET is operating at full load current during phase C, the proposed method will utilize the device current during phase B to avoid self-heating due to excessive switching loss. The device current during the saturation region is temperature dependent, as given by\(^{(15)}\)

\[
I_{D,sat}(T) = \frac{\mu(T) C_{ox} Z}{2L} \left| V_{GS} - V_{th}(T) \right|^2 \left( \frac{L}{L - \Delta L} \right)
\]

(1)

where \(\mu\) is the carrier mobility, \(Z\) is the channel length reduction subject to increase drain-to-source voltage due to depletion and \(T\) is temperature. The quadratic term in (1) implies that \(I_{D,sat}(T)\) exhibits non-linear temperature dependence.

A linear temperature dependence can be found by taking the square root of the saturation current, as given by

\[
\sqrt{I_{D,sat}(T)} = k \sqrt{\mu(T)} \left| V_{GS} - V_{th}(T) \right| \quad \text{ (2)}
\]

where \(k = \sqrt{\frac{C_{ox} Z}{2L \Delta L}}\).

Since the device is not fully turn-on, the temperature effect on \(\mu\) can be neglected, as compared to the temperature effect on \(V_{th}\)\(^{(14)}\). Thus, the temperature dependence of \(\sqrt{I_{D,sat}(T)}\) is dominated by \([V_{GS} - V_{th}(T)]\), and is expected to have linear increments as temperature rises, as \(V_{th}\) has a negative temperature coefficient.

Threshold voltage can be extracted with two sets of saturation currents \(I_{D,sat1}\) and \(I_{D,sat2}\) that biasing with known gate-to-source voltage \(V_{GS1}\) and \(V_{GS2}\), respectively. Under the same temperature condition, the terms \([\mu(T) C_{ox} Z]/2L\) and \(L/(L - \Delta L)\) in equation (1) can be eliminated by dividing \(I_{D,sat2}\) by \(I_{D,sat1}\):

\[
\frac{I_{D,sat2}}{I_{D,sat1}} = \frac{V_{GS2} - V_{th}}{V_{GS1} - V_{th}} = a \quad \text{ (3)}
\]

By solving equation (3), the threshold voltage at the specific temperature can be obtain as follows:

\[
V_{th} = aV_{GS1} - V_{GS2} \quad \text{ (4)}
\]

where \(a = \sqrt{I_{D,sat2}/I_{D,sat1}}\).

2.2 Multi-level Gate Control Method A multi-level gate control method is proposed to obtain the device saturation current as illustrated in Fig. 2. When junction temperature (\(T_j\)) monitoring is not needed, the gate-to-source voltage is controlled at normal mode operation, where \(V_{GS}\) is switching between nominal turn-on/turn-off voltages \((V_{GS,on}, V_{GS,off})\). When junction temperature information is desired, the gate-to-source voltage is operating at test mode. If junction temperature is estimated based on \(\sqrt{I_{D,sat}}\), 1-step gate control is applied, where a test voltage \(V_{GS, sat}\) is generated during the saturation region for saturation current measurement. If junction temperature is estimated via \(V_{th}\), 2-step gate control is utilized. In this case, two test voltages \((V_{GS1}, V_{GS2})\) will be generated during the saturation region. The corresponding saturation currents can be obtained
Multi-level gate control is achieved by adding a multi-level output (MLO) generation block to the conventional isolated gate driver, as illustrated in the clamped inductive load configuration shown in Fig. 3. The MLO generation block is inserted between node A and G of the turn-on gate resistor path so that the minimum change is made on the traditional driving scheme. The gate-to-source voltage is supplied either by the conventional gate driver or the MLO generation block, depending on whether test mode is enabled. Three switches, S1 to S3, are controlled by test_ctrl, Vtest_ctrl and Vadj_ctrl, respectively. Test mode is enabled/disabled by switching S1 off/on. S2 is inserted to prevent current shoot-through between the transitions of VGS supply. S3 is for VGS level control.

Detailed operation is illustrated with 2-step gate control as shown in Fig. 4. When test mode is enabled (test_ctrl is high) while S2 is not turned on yet (Vtest_ctrl is low), VGS is slowly pulled to AVSS through resistor RGS. Then, VGS is set to VGS1 by turning S2 on (Vtest_ctrl is high) while S3 remains off (Vadj_ctrl is low), and the corresponding device current ID_sat1 is recorded. Finally, VGS is set to VGS2 by turning S3 on (Vadj_ctrl is high) to capture another saturation current ID_sat2. The two test voltages are given by:

\[
\begin{align*}
V_{GS1} &= V_{ref} - V_s, \\
V_{GS2} &= \left(1 + \frac{R_1}{R_2}\right)V_{ref} - V_s
\end{align*}
\]

The normal operation can be resumed once the settled current information is captured. Finally, the Vth at a preset temperature can be obtained with the measured saturation currents and the two sets of test voltages described in (5) by equation (4).

All the switches in the MLO generation block should not switch at the same time to prevent current shoot-through. When \(\sqrt{ID_{sat}}\) is adopted as the junction temperature estimator, 1-step gate control can be achieved by simply disable Vadj_ctrl. The test time is shorter compared to 2-step gate control.

3. Concept Validation

The multi-level gate control method is validated by double pulse clamped inductive load testing, which emulates the switching operation of a SiC power MOSFET. Figure 5 shows the measurement setup based on the schematic shown in Fig. 3. A discrete SiC power MOSFET M_SiC (C2M0080120D, Cree Inc.) is fixed on top of a heatsink and the temperature is controlled by placing it on a hotplate (UC150, Smart). The preset temperature is read by an analog temperature sensor (LMT86, Texas Instruments), which is placed adjacent to M_SiC.

A 246 \(\mu\)H inductor is chosen as a load (\(L_{load}\)), and a SiC Schottky diode (C4D20120A, Cree Inc.) is used as a free-wheeling diode (\(D_J\)). The MLO generation block and the conventional gate driver are designed on separated printed circuit boards (PCBs) for flexibility. The device current is measured by a Rogowski coil (CW7Mini HF06B, PEM) with sensitivity of 50 mV/A. The measured current can be either observed by an oscilloscope or processed by data acquisition system directly. Oscilloscope (MDO4104B-3, Tektronix) is adopted here for demonstration purpose.

The two test voltages VGS1 and VGS2 are designed to meet the saturation region criteria. It is desired to have gate-to-source voltage slightly higher than threshold voltage to avoid excessive switching loss. Here, VGS1 and VGS2 are designed to be 3.86 V and 4.68 V, respectively. Figure 6 shows the double pulse testing waveforms at room temperature. For the ease of observation, the timing periods of VGS1 and VGS2 are...
set to be relatively longer than the time required for current to settle. It can be observed that the actual current settling time is around 3 μs. In practical applications, device temperature can be estimated as long as the current settling time is well covered by clock duty time. For example, the current settling time can be sufficiently covered by a clock with switching frequency up to 50 kHz with 50% duty cycle.

Double-pulse test is performed at least 30 minutes after the temperature is set to allow MSiC to reach thermal equilibrium, where the junction temperature can be assumed to be that of the hotplate. Soft turn-on is designed to avoid drastic current change for fast settling. In this demonstration, saturation current is obtained by averaging 5000 data points captured by oscilloscope right before \(V_{GS}\) transition points as indicated by the black bars in Fig. 6. Five measurements are taken to average out the random error contributed by oscilloscope. Figure 7 summarizes the results together with the mean threshold voltage calculated from the five measurements at each temperature setting. The results show small variations among the five measured data at each preset temperature. The mean threshold voltage and its linear fit are plotted in Fig. 8 together with the \(V_{th}\) extracted from the datasheet \(^{16}\). Both curves show similar negative temperature dependency. The temperature sensitivity of the measured data shows close agreement with the datasheet.

Next, the temperature dependence of the square root of the saturation current at the two test voltages are examined. The measured \(\sqrt{I_{D,sat}}\) at \(V_{GS1} = 3.86 \text{ V}\) and \(\sqrt{I_{D,sat}}\) at \(V_{GS2} = 4.68 \text{ V}\) are plotted in Fig. 9 and Fig. 10, respectively, together with the respective mean values. All five measurements have shown positive temperature dependence with excellent linearity, which suggest the promising applicability for effective temperature monitoring.

### 4. Junction Temperature Monitoring on Boost Converter

To evaluate the online temperature monitoring potential of the proposed method, a boost converter operates at continuous-conduction mode (CCM) is built based on the schematic shown in Fig. 11, with \(L = 0.5 \text{ mH}\), \(C_{\text{load}} = 100 \mu \text{F}\)
and $R_{\text{load}} = 10 \, \Omega$. A Schottky diode with part number of C4D20120A is adopted as $D_s$ and a brand new SiC power MOSFET with part number of C2M0080120D is adopted as the power device $M_{\text{SiC}}$ under junction temperature monitoring.

Figure 12 shows the actual implementation of the boost converter. Similar to the concept validation setup shown in Fig. 5, $M_{\text{SiC}}$ is fixed on top of a heatsink, which is placed on a hotplate surface. Through temperature control of the hotplate, the junction temperature rise of $M_{\text{SiC}}$ due to ambient condition is emulated. An analog temperature sensor (LMT70, Texas Instruments) is attached to the heatsink surface in adjacent to $M_{\text{SiC}}$ for heatsink temperature measurement. A voltage measurement circuit with embedded isolation feature (isolated voltage monitor, IVM) is incorporated for on-state voltage measurement.

As $\sqrt{I_{D,\text{sat}}}$ has the advantage of easier testing compared to $V_{th}$, junction temperature monitoring is achieved by 1-step gate control in this demonstration.

### 4.1 $\sqrt{I_{D,\text{sat}}}$ Dependence of Junction Temperature

Before online junction temperature monitoring is performed, the $\sqrt{I_{D,\text{sat}}}$ dependence of junction temperature has to be characterized. The variation of $\sqrt{I_{D,\text{sat}}}$ with junction temperature at a chosen $V_{GS}$ can be either calibrated from double pulse testing, as described in Section 3, or from the transfer characteristic curves measured by an $I$-$V$ curve tracer. The latter method is adopted in this demonstration as it is a more general solution.

Figure 13 shows the dependence of device current on $V_{GS}$ at various junction temperatures measured by an $I$-$V$ curve tracer (Tektronix 371A). Based on the measurement, the $\sqrt{I_{D,\text{sat}}}$ dependence of junction temperature at any given $V_{GS}$ can be obtained and modeled by a least-square linear fit, as given by

$$T_j = a \sqrt{I_{D,\text{sat}}} + b \quad \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdots \cdOTS
modeled by the channel length modulation parameter \( \lambda \). By assuming \( \Delta L \ll L \), the term \( L / (L - \Delta L) \) in equation (1) can be approximated to \((1 + \lambda V_{DS})\), where \( \lambda V_{DS} = \Delta L/L \).

Based on equation (1), the influence of \( V_{DS} \) is accounted by substituting \( \sqrt{I_{DS}} \) in equation (6) with

\[
\sqrt{I_{DS,\text{sat}}} = \sqrt{\frac{1 + \lambda V_{DS,\text{sat}}}{1 + \lambda V_{DS,\text{meas}}}} I_{D,\text{meas}} \tag{7}
\]

where \( V_{DS,\text{sat}} \) is the drain-to-source voltage set during the calibration process, \( V_{DS,\text{meas}} \) and \( I_{D,\text{meas}} \) are the actual drain-to-source voltage and saturation current measured. With known \( \lambda \), junction temperature can be estimated at any measured \( V_{DS} \) with the following equation:

\[
T_j = a \sqrt{\frac{1 + \lambda V_{DS,\text{cal}}}{1 + \lambda V_{DS,\text{meas}}}} I_{D,\text{meas}} + b \tag{8}
\]

The parameter \( \lambda \) can be pre-characterized by I-V curve tracer. By re-arranging equation (7), \( \lambda \) can be calculated with equation (9).

\[
\lambda = \frac{k - 1}{V_{DS,\text{meas}} - k V_{DS,\text{cal}}} \tag{9}
\]

where \( k = I_{D,\text{meas}}/I_{D,\text{sat}} \). \( I_{D,\text{meas}} \) is obtained at a known \( V_{DS,\text{meas}} \), and with the same \( V_{GS} \) and temperature settings as \( I_{D,\text{sat}} \) that measured at \( V_{DS,\text{sat}} \).

Figure 15 illustrates the influence of channel length modulation correction, where the temperature dependence of \( I_{D,\text{sat}} \) measured at \( V_{DS} = 10 V \) and 15 V, respectively, with \( V_{GS} = 3.5 V \) and 4V are shown. Due to channel length modulation effect, \( I_{D,\text{sat}} \) measured at \( V_{DS} = 15 V \) are slightly higher than that of \( V_{DS} = 10 V \). Without correction, it will result in overestimation of junction temperature if the actual operating \( V_{DS} \) is higher than 10V. By taking square on both sides of equation (7), the temperature dependence of \( I_{D,\text{sat}} \) measured at \( V_{DS} = 10 V \) is corrected to that of \( V_{DS} = 15 V \), as shown by dashed lines in Fig. 15. The results have shown a close match with the measured data.

### 4.2 Experimental Results

For the ease of demonstration, test mode is applied to every clock cycles. \( V_{GS} \) is stepped up from the nominal turn-off voltage to 3.86V for saturation current measurement at each turn-on transition. The boost converter is operating at 20kHz switching frequency and 40% duty cycle, with input voltage \( V_{DC} \) fixed at 10V.

Since the duty cycle is fixed, the boost converter will reach a thermal steady-state after output voltage stabilized. After power up, the boost converter is operating at room temperature first for > 10 minutes to allow it to reach the thermal steady-state. Then, the hotplate is turned on to emulate the ambient condition with high temperature. A longer operation time is allowed to let both the hotplate and boost converter to reach their thermal steady-state, follows by 8 cycles of saturation current and on-state voltage measurements. The hot-plate temperature is changed for a few times to observe the changes at different ambient conditions. For further investigation, the junction temperature is estimated via on-state resistance \( R_{\text{(on)}} \) as well for comparison with the proposed method. The temperature dependence of \( R_{\text{on}} \) is device current dependent, which can be calibrated by I-V curve tracer as well. Figure 16 shows the corresponding surface model.

Figure 17 shows the measured device current and the on-state voltage at different heatsink temperatures \((T_s)\) of one
system noise, and the successful extraction of threshold voltage \( V_{th} \). The proposed method provides flexibility on choosing load independent temperature estimator from \( \sqrt{I_{D,\text{sat}}} \) and \( V_{th} \), where \( \sqrt{I_{D,\text{sat}}} \) has the advantage of a shorter test time and hence, suitable for timing-critical applications. The experiment has demonstrated the feasibility of the proposed method for junction temperature monitoring on a live system. It also suggests the potential of the proposed method as an aid for future development of EHM system.

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Junction Temperature Estimation via Turn-on Saturation Current Measurement (Hui-Chen Yang et al.)


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