Silicon carbide (SiC) devices are considered as key enablers for the development of highly efficient and compact dc-dc converters for low- and medium-voltage applications. Besides their high temperature capability and low conduction losses, they provide superior switching characteristics. This paper emphasizes the design challenges of SiC devices in the low- and medium-voltage ranges arising from their fast switching speeds. First, detailed measurement results on the switching characteristics of 1200 V SiC devices and the different leakage inductances are presented. The results are assessed with regard to the switching losses as well as the transient voltage and current overshoots. The impact on the switching behavior as a function of leakage inductances is shown. The leakage inductances also influence the resonance frequency of the power module and dc-dc converters. The determination of the size of the EMI filters is a crucial design aspect. Its significance is demonstrated using an 800 V dc-dc converter with commercially available SiC MOSFETs. In addition, zero-voltage switching is emphasized to reduce the impact of the parasitic elements of the module on the switching behavior. However, the performance of 10 kV SiC MOSFETs in a medium-voltage dc-dc converter shows that a significant amount of commutation energy is required to ensure a successful soft-switching transition.

**Keywords:** silicon carbide, MOSFETs, converters, switching transients

1. **Introduction**

Power electronic converters are being used throughout all low- and medium-voltage applications. They are the key technology for renewable energies, electrical traction systems and future dc grids [11][16]. To develop highly efficient and compact dc-dc converters for low- and medium-voltage applications, the advantages of wide-bandgap (WBG) devices are particularly crucial [7][8]. It is generally assumed, that WBG power semiconductors enable a volume and cost reduction of converters due to higher switching frequencies and thus power semiconductors formation. Furthermore, the impact on the filter design is shown as a function of the leakage inductances. The leakage inductances also influence the resonance frequency of the power module and dc-dc converters. The determination of the size of the EMI filters is a crucial design aspect. Its significance is demonstrated using an 800 V dc-dc converter with commercially available SiC MOSFETs. In addition, zero-voltage switching is emphasized to reduce the impact of the parasitic elements of the module on the switching behavior. However, the performance of 10 kV SiC MOSFETs in a medium-voltage dc-dc converter shows that a significant amount of commutation energy is required to ensure a successful soft-switching transition.

This paper emphasizes design challenges of silicon carbide (SiC) semiconductors in the low and medium-voltage range arising from their fast switching speeds. Instead of the already well known issues about the required high common mode rejection ratio (CMRR) of the controller, the gate circuitry and the measurement units [10][11], this contribution focuses on the design challenges arising from the filter design. It is shown, that the leakage inductances of SiC power modules, together with their metal-oxide semiconductor field-effect transistor (MOSFET) output capacitance, create a resonant tank, which is the source for disturbance in the EMI spectrum of converters [12]. Due to an increased excitation of the resonant frequencies, high-frequency disturbances are appearing in the frequency spectrum. This is a crucial design aspect to determine the size of the EMI filters. The analysis is based on detailed investigations on the leakage inductance of the switching cell and the switching characteristics of 1200 V SiC devices. The results are assessed with regard to the resonant frequency as well as the transient voltage and current overshoots. The influence on the switching behavior is shown as a function of the leakage inductance. Furthermore, the impact on the filter design is demonstrated based on an 800 V dc-dc converter using a commercially available SiC MOSFET power module.

The stray inductance of SiC medium-voltage dc-dc converters cannot always be reduced in the same manner as for low-voltage applications due to higher clearance requirements. Therefore, soft-switching converter topologies and operation strategies are envisaged to reduce switching losses and filter size. Achieving zero-voltage switching in medium-voltage SiC converters, however, requires a careful converter design as well as a precise control of the voltage and current waveforms to provide sufficient commutation energy during the switching transitions.

2. **Influence of Stray Inductance on the Switching Behavior**

The stray inductances \( L_{\text{module}} \) of the power module in combination with the output capacitance \( C_{\text{oss}} \) of the SiC MOSFETs form a resonant circuit. Using an exemplary low-voltage power module (CCS050M12CM2 [20]) which employs 1200 V MOSFETs (CPM2-1200-0025B), the resonant
The voltage response of a current pulse is determined experimentally using a frequency $f_{\text{res}}$ and voltages $U_{\text{L}}$. The total power-loop inductance, including the stray inductance $L_{\text{loop}}$, is plotted against the jumper inductance of the total power-loop inductance, measured at bipolar transistors (IGBTs) $L_{\text{loop}}$. In the following, the influence of the stray inductance on the switching transients is investigated experimentally using a half-bridge setup with a variable stray inductance $L_{\text{loop}}$. The adjustable range of the variable inductance is from 0 to 35 nH, which is approximated by the cut-off frequency $f_{\text{c}}$ of a first order low-pass filter:

$$f_{\text{c}} = \frac{1}{2\pi \sqrt{L_{\text{loop}} C_{\text{oss}}}} = \frac{1}{2\pi \sqrt{30 \text{nH} \cdot 220 \text{pF}}} = 62 \text{MHz}.$$ 

These voltage slopes are at least one order of magnitude higher compared to the switching slopes of insulated-gate bipolar transistors (IGBTs) $U_{\text{IGBT}}$. In the following, the influence of the stray inductance on the switching transients is investigated experimentally using a half-bridge setup with a variable stray inductance $L_{\text{loop}}$.

### 2.1 Hardware Setup

A switching cell with an adjustable power-loop stray inductance $L_{\text{loop}}$ is developed according to the schematic shown in Fig. 1. The variable inductance $L_{\text{loop}}$ is realized using different jumper positions of a pin header, as shown in a functional sketch of a low and high value inductance in Fig. 2. The adjustable range of $L_{\text{loop}}$ is 1 nH to 20 nH, which is determined experimentally using the voltage response of a current pulse $i(t)$ given in (20-21). The measured inductance of the total power-loop inductance, measured at the dc-link capacitor terminals, is plotted against the jumper position in Fig. 3. The total power-loop inductance $L_{\text{loop}}$ includes the stray inductance $L_{\text{stray}}$ and the inductance of the current viewing resistor (CVR) $L_{\text{CVR}}$:

$$L_{\text{loop}} = L_{\text{stray}} + L_{\text{CVR}}.$$  

To design the included CVR (SDN-414-10) with a contacting inductance $L_{\text{CVR}} = 7$ nH and the printed circuit board (PCB) layout, a minimum power-loop inductance of $L_{\text{loop}} = 25$ nH is reached. A photograph of the PCB is shown in Fig. 4.

The switching transients of the low-side switch $S_2$ are recorded using the double pulse test bench as published in (26-27). The employed power MOSFETs are 1200 V devices from Cree (C2M0025120D). Furthermore, a careful setup of the measurement probes is chosen to respect the guidelines given in (28).

### 2.2 Measurement Results

First, the impact of the power-loop inductance on the switching behavior is investigated. The turn-on event waveforms of the low-side switch $S_2$ and the high-side diode are plotted in Fig. 5 at a dc-link voltage of $U_{\text{dc}} = 400$ V and a load current of $I_S = 100$ A. A high voltage overshoot ($\approx 100\%$) and a significant ringing is observed in the high-side switch (i.e., free-wheeling diode) voltage $u_{\text{Diode}}$. A similar ringing is observed in the low-side source current $i_S$ with a significant overshoot ($\approx 50\%$). Analogously, the transient turn-off waveforms are plotted in Fig. 6. A high voltage overshoot ($\approx 50\%$) is observed across the low-side switch voltage $u_{\text{DS}}$, while the source current $i_S$ and the switch voltage $u_{\text{DS}}$ show an equal ringing.

Secondly, the oscillation frequencies of $a_{\text{osc}}$, and $a_{\text{off}}$ during the switching events are extracted from all the conducted measurements. Their dependency on the loop inductance $L_{\text{loop}}$ as a function of the switched current $i_S$ is shown in Fig. 7 and as a function of the dc-link voltage $U_{\text{dc}}$ in Fig. 8. Figure 7 shows that the resonant frequencies are independent of the load current $I_S$ of the switching cell. However, Fig. 8 clearly shows the dependency of the resonance frequency on

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**Fig. 1.** Schematic with adjustable inductance $L_{\text{loop}}$

**Fig. 2.** Functional sketch of the variable inductance using a pin header

**Fig. 3.** Measured inductance depending on jumper position

**Fig. 4.** Demonstrator PCB, top view
the dc-link voltage $U_{dc}$. This effect results from the voltage dependent output capacitance $C_{oss}$ of the MOSFET$^{(20)}$.

3. Filter Design

In the following, the impact of the SiC module’s resonant frequency on the EMI characteristic and the filter design of a low-voltage dc-dc converter is analyzed. The analysis is carried out for a bidirectional interleaved multi-phase synchronous boost converter, as pictured in Fig. 9, with a switching frequency of $f_{sw} = 150$ kHz, a nominal output power of $P_{out} = 42$ kW and nominal input and output voltages of $U_{in} = 400$ V and $U_{out} = 800$ V. The converter utilizes a commercially available SiC module (CCS050M12CM2 from Wolfspeed$^{(20)}$), which is based on the EconoPack 2 package, which was originally developed for silicon (Si) IGBT semiconductors. Therefore, the module’s loop inductance of $L_{loop}^{pcb} \approx 30$ nH is not optimized for SiC applications$^{(20)}$.

The high $\frac{dv}{dt}$ voltage slope at the switching node SW, which is essential for an efficient hard-switched converter, excites the resonant circuit consisting of the output capacitance $C_{oss}$ and the stray inductance $L_{loop}^{pcb}$. In contrast to Si-based converters, where the module resonance is not exited by the slow switching slopes, the SiC-based hard-switching converter needs a second wide-band high-frequency EMI filter, which attenuates the module’s resonant frequency.

3.1 Measurements and Criteria for EMI Filters

Figure 10 shows the conducted emission of the 3-phase dc-dc converter at 2 kW using different filter elements. The switching frequency of 150 kHz together with its harmonics and the resonant frequency of the module, which has its peak at 30 MHz, is plotted in Fig. 10. The third harmonic of the switching frequency is visible at 450 kHz. Due to the interleaved operation of the 3 phases, the effective switching
frequency is located at 450 kHz, which leads to an increase of the peaks at 450 kHz and 1.05 MHz and other odd harmonic frequencies of 150 kHz and 450 kHz. Therefore, a common mode choke “CM1” with an attenuation-peak between 400 kHz and 2 MHz was selected for the first filter stage, see Fig. 12.

The green curve depicts measurement results using Y-capacitors with \( C_y = 330 \text{nF} \) and the commercially available common-mode choke “CM1” which is shown in Fig. 11(a). The common mode choke “CM1” (Kaschke 048.096) provides a distinctive attenuation in the sub-5 MHz region. Since the converter is a laboratory prototype, no specific electromagnetic compliance (EMC) limits were imposed. A general limit of 70 dB \( \mu \)V was set for example purposes. For an application outside of academia it is recommended to set the switching frequency below 150 kHz (e.g., 144 kHz), so that the amplitude of the switching frequency is not visible in the conducted emissions. To further attenuate the module resonance at 30 MHz, a second common-mode filter with a different frequency range has to be applied. Therefore, a prototype common-mode choke (“CM2”, see Fig. 11(b)) with a peak-attenuation at 30 MHz and a wide absorbing range from 10 MHz to 70 MHz is implemented using a toroidal ferrite (Würth 74270191) with four turns. Combining both common-mode chokes, “CM1” and “CM2”, results in a nearly constant impedance over a broad frequency range as shown in Fig. 12. A conducted noise-emission plot (black curve) with the newly developed “CM2” choke to attenuate the module’s resonant frequency is shown in Figure 10. The second filter stage, consisting of “CM2”, leads to a greatly reduced emission in the upper frequency band. In comparison to the “CM1” choke (80 dB \( \mu \)V (= 10 mV) at 30 MHz), the “CM2” choke (67 dB \( \mu \)V (= 2.24 mV) at 30 MHz) provides a 13 dB higher attenuation at 30 MHz, due to an impedance increase from 380 \( \Omega \) (“CM1”) to 1.7 \( \Omega \) (“CM2”).

This results in a 4.47 times lower voltage-ripple and the interference-power is reduced by a factor of 20. Since the impedance of the choke “CM2” at 30 MHz is also higher by a factor of 4.47 compared to the impedance of the choke “CM1”, the measured module resonance emission shows only a common-mode noise component. Otherwise, if the module resonance would have a differential-mode noise component, the measured voltage-ripple reduction of 4.47 times would not correspond to the increased common-mode impedance of the choke “CM2” by the factor 4.47.

### 3.2 Volume Impact of EMI Filters

The additional EMI filter increases the overall volume of the aforementioned dc-dc converter by 21% and, hence, strongly contributes to the overall volume and costs of the converter.

This becomes even more crucial for medium-voltage dc-dc converters using SiC devices. Although the output capacitance of SiC devices decreases with higher blocking voltages, the overall leakage inductance of the module and the commutation cell potentially increases as a result of the required clearance and creepage distances. Therefore, the module resonances of medium-voltage SiC modules and switching cells are expected to be in the same range as of low-voltage dc-dc converters. Moreover, the EMI filters have to withstand the high dc-link voltages and, hence, become more costly and bulky.

### 4. Zero-Voltage Switching

Soft-switching topologies and operation strategies are a means to reduce the impact of the module’s parasitic elements on the switching behavior\(^{(3)}\). By shaping the \( \Delta v/\Delta t \) and \( v/\Delta t \) during the switching transitions, the switching losses and the EMI can be influenced. This provides the opportunity to develop highly efficient and compact medium-voltage dc-dc converters which can be used as flexible power routers in medium-voltage applications, e.g., for the interconnection of future dc grids\(^{(3)}\)(30–32).

Figure 13 depicts a zero-voltage turn-on switching transition of a 10 kV SiC MOSFET from Wolfspeed operated in a three-phase triple-active bridge (3ph-TAB) converter at a dc-link voltage of 2.5 kV\(^{(30)}\). The blue curve corresponds to the voltage \( v_{\text{DS}} \), which is measured across the switch \( S_2 \) (see Fig. 1) at one phase leg of the 3ph-TAB converter. The corresponding load current \( i_L \) is shown in red. Please note that the amplitude and the slope of the load current during the switching event are mainly determined by the operating point.
and the operation strategy of the 3ph-TAB converter\(^{(32)(33)}\). Moreover, the oscillations of the load current are caused by a resonant circuit, which results from the parasitic elements of an externally connected transformer and inductor. Both components, the transformer and the inductor, form the leakage inductance, which is the main energy transfer element of a 3ph-TAB converter.

Once \(S_1\) is turned off, the load current \(i_L\) charges the output capacitance \(C_{\text{oss}}\) of \(S_1\) and discharges the one of \(S_2\), respectively (see Fig. 1). Consequently, the voltage slope during turn-off is mainly determined by the load current \(i_L\) and the output capacitances \(C_{\text{oss}}\) of the semiconductors. The output capacitances \(C_{\text{oss}}\) of the 10 kV SiC MOSFETs are highly non-linear and range from 16 nF at \(V_{\text{DS}} = 1\) V to 100 pF at \(V_{\text{DS}} = 2.5\) kV\(^{(34)}\). At \(V_{\text{DS}} = 1\) kV, \(C_{\text{oss}}\) equals approximately 160 pF. Despite the relatively low values of \(C_{\text{oss}}\), the required commutation energy \(E_{\text{com}}\) at dc-link voltages of 2.5 kV ... 5 kV is in the range of 0.6 mJ ... 2.5 mJ, which is due to the quadratic contribution of the dc-link voltage: \(E_{\text{com}} = \frac{1}{2} \cdot 2C_{\text{oss}} \cdot U_{\text{dc}}^2\). Therefore, the load current is mostly used for the commutation process and the current in the channel of the SiC MOSFET is cut-off much faster\(^{(35)}\) than implied by the waveforms. This resembles the behavior of turn-off snubber capacitors in low-voltage applications. The given load current of approximately 2.5 A leads to a \(di/dt\) of only 8 kV/\(\mu\)s. At higher switching currents (5 A ... 6 A) the voltage slope exceeds 25 kV/\(\mu\)s. After the dead time, which is 1.5 \(\mu\)s, the switch \(S_2\) is turned on under zero-voltage switching conditions. Due to the controlled \(di/dt\) and the soft turn-on transition, the switching losses and the EMI are reduced.

The rms current, which is required to ensure soft-switching during the commutation process is approximated by

\[
\frac{2 \cdot E_{\text{com}}}{T_{\text{dead}} \cdot U_{\text{dc}}} = \frac{2 \cdot 5.6 \text{ mJ}}{1.5 \mu\text{s} \cdot 2500 \text{ V}} = 0.32 \text{ A}
\]

\[
U_{\text{dc}} = \frac{2 \cdot 2.5 \text{ mJ}}{1.5 \mu\text{s} \cdot 5000 \text{ V}} = 0.66 \text{ A}
\]

assuming a constant current during the dead time, a dead time of \(T_{\text{dead}} = 1.5 \mu\text{s}\) and a linear drain-source voltage drop but neglecting the output capacitance increase at low drain-source voltages. At a target dead time of 500 ns, the required rms current is approximately 1 A ... 2 A. This, however, equals more than 10% of the nominal dc-current capability of the 10 kV SiC MOSFETs at a junction temperature of 150 °C.

If the rms value of the load current drops below the required threshold, the output capacitor of the switch \(S_2\) cannot be discharged completely during the dead time. This results in a quasi hard turn-on switching as shown in Fig. 14(a) and Fig. 14(b). Given a constant rms current of only 0.2 A, the voltage across \(S_2\) is still at 2 kV at the end of the dead time, see Fig. 14(a). Besides providing a sufficient amount of commutation energy, zero-current crossings must be avoided during the dead time. This is shown in Fig. 14(b), where the load current slowly decreases from 1.1 A to −0.3 A during the commutation process. As long as the load current is positive, the output capacitor of the 10 kV SiC MOSFET is discharged. If the current crosses zero, however, the output capacitor gets charged again, which partially negates the previous commutation process. At the turn-on instant of \(S_2\), the charge stored in the output capacitor \(C_{\text{oss}}\) is dissipated within the switch \(S_2\). This results in significant turn-on losses and a high \(di/dt\).

The measurements show, that a significant amount of commutation energy has to be provided by the load current to ensure a successful zero-voltage turn-on process. To address this issue, the load current during the switching event has to be adjusted, e.g., by altering the operation strategy\(^{(35)(36)}\), by adjusting the turns-ratio of the transformer\(^{(37)}\) or by injecting reactive power such that a certain switching current is guaranteed. Moreover, a variable dead time in conjunction with a zero-current detection could be used to detect the end of the commutation process\(^{(36)}\).

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\begin{figure}[h]
\centering
\includegraphics[width=\linewidth]{fig13.png}
\caption{Zero-voltage turn-on transition of a 10 kV SiC MOSFET operated in a 3ph-TAB converter}
\end{figure}

\begin{figure}[h]
\centering
\includegraphics[width=\linewidth]{fig14.png}
\caption{Quasi hard turn-on transition of 10 kV SiC MOSFETs operated in a 3ph-TAB converter}
\end{figure}
5. Conclusions

The influence of the stray inductance of the power device packaging on the switching behavior has been investigated using different prototype switching cells. Furthermore, it has been shown that the parasitic inductances of the module have a significant effect on the EMI of wide-bandgap SiC dc-dc converters. The impact on the filter design has been discussed using the example of a 42kW dc-dc converter prototype with high power density. Two common-mode filters with different frequency ranges have been applied to attenuate the high-frequency noise emitted by the converter. This has a significant impact on the overall volume and costs of future SiC dc-dc converters. Thus, in modern, high-density SiC power converters, the design of the semiconductor package cannot be decoupled anymore from the overall converter or system design. Furthermore, zero-voltage switching has been emphasized on the example of a 10 kV 3ph-TAB as a basis for system design. Furthermore, zero-voltage switching has also been shown to be a prerequisite for the successful operation of two common-mode filters. Due to the high-frequency noise emitted by the converter, this is particularly crucial, as the required load current is more than 10% of the nominal current rating of the 10 kV SiC MOSFETs.

Acknowledgment

The work for this paper has been carried out within the scope of several research projects, namely the postgraduate program “mobileEM” (GRK 1856) of Deutsche Forschungsgemeinschaft (DFG), the research project “Research Campus Future Electrical Networks” (FEN) (03SF0489) and the research project HV-ModAL (16EMO0105), both funded by the German Federal Ministry of Education and Research (BMBF), and in close cooperation with Ford Motor Company.

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Design Challenges of SiC Devices for DC-DC Converters (Georges Engelmann et al.)


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