An Optimization Design for Transformer and Output Filter of a Micro-inverter with Passive Integration Technique

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The transformer and output filter of the micro-inverter usually have a considerable footprint in the total system. In order to improve the power density of a micro-inverter, an integrated structure of passive components including transformer and output filter is proposed with flexible multilayer foils (FMLF). The topology of the micro-inverter is modified, which enables the integration of these passive components. In this paper, the design of the integrated structure is detailed. The distributed components model of the structure is established to verify the performance of the flexible foils. Finally, a prototype of the proposed structure is built and used in the micro-inverter. Experimental results are included to verify the integration design.

Keywords: power density, passive integration, transformer, output filter

1. Introduction

The passive components in a micro-inverter, such as the output filter and the transformer usually take up considerable space in the total system. If the transformer and the output filter can be integrated into one unit, the volume occupied by these passive components will be decreased. Moreover, the drawbacks of the parasitic effects caused by lead wire between the discrete components can be reduced.

Passive integration is such a technique which can gather together the passive components including inductive components and capacitive components, and thereby the volume will be optimized. The Flexible Multilayer Foil (FMLF) integration technique and the Printed Circuit Board (PCB) integration technique are usually adopted for passive integration.

With regards to FMLF technique, the principle and the structure of the FMLF are shown in Fig. 1. A dielectric layer is inserted between two conductive layers, creating capacitance. While, the conductive layers can be used as windings, creating inductance, thus, the inductor and the capacitor are generated simultaneously in the same structure. This technique was initially used to integrate a resonant chamber (1), and then it was used to integrate the EMI filters (2)–(5) in power converters. A boost inductor and an EMI filter are integrated with this technique (6) (7) in a PFC circuit. Later, an improved structure with FMLF in a modified PFC circuit was proposed to further reduce the volume of the EMI filters in (8) (9). An integrated structure with the FMLF technique is presented in (10) to integrate the transformer, the leakage inductor and the parallel inductor in a LLC converter.

In this paper, an integrated structure using the FMLF technique is presented to integrate the transformer and the output filter of a micro-inverter. The circuit is modified for integrating the passive components. The design procedure of the integrated structure is provided. The distributed components model of the structure is established and applied to verify the performance of the FML foils. Finally, the prototype of the proposed integrated structure is explored and used in a 100 W micro-inverter. The experimental results are provided to verify the design.

2. Integrated Structure Design

2.1 Modified Micro-inverter for Passive Components Integration

Topology of the micro-inverter is shown in Fig. 2, which consists of a fly-back converter, an unfolding bridge, and an output filter. The fly-back converter generates half-wave sinusoidal waveforms on the pseudo DC link, and then the unfolding bridge works with line frequency to unfold the output waveforms of the fly-back converter to sinusoidal waveforms.

In the positive and negative half utility cycle, the operation stages of the secondary side of the micro-inverter are shown in Figs. 3(a) and (b), respectively (11).

When the output filter is moved forward as shown in Fig. 4, the operation stages of the circuits in Figs. 3 and 4 is same.
The only difference between these two circuits is that the output filter in Fig. 4 becomes a DC side filter.

Thus, the transformer and the output filter in the modified micro-inverter for the passive integration is presented in Fig. 5. The grid filter $L_o$ is moved forward and located between the secondary side of the transformer and the unfolding bridge (12) (13).

### 2.2 Integrated Structure

In Fig. 6(a), a FML foil named F1 with typical structure is presented. The integrated foil have four layers which are two conductive layers with bronze color, one white insulation layer, and a blue dielectric layer. The conductive layers themselves can be used as inductors (or transformer), which can also be performed as the plates of a planar capacitor. The dielectric film is inserted between two conductive layers for creating the capacitance. The insulation layer adhered to one conductive layer (i.e. 1st). Then, inductance and capacitance are integrated into the same unit.

When different terminals of the FML foil are connected to outer circuit, different equivalent circuit can be obtained as shown in Fig. 6(b). As can be seen, when terminals $a$, $c$ are chosen to connect to outer circuit, the foil can be used as an inductor. The foil can be performed as a capacitor when terminals $c$ and $d$ are connected. When terminals $a$, $c$ and $d$ of the winding are connected to external circuit, it can be used as a low pass filter (14).

According to the equivalent circuit of the FML winding F1, then, another conductive layer and insulation layer are attached to winding F1 as shown in Fig. 7. The 2nd and 3rd conductive layers can be used as a transformer, where the 3rd conductive layer can be used as the primary side winding of the transformer, and the 2nd conductive layer is employed as the secondary side winding. Furthermore, the 1st and 2nd conductive layers along with the dielectric film form an integrated capacitor. The length of these three conductive layers can be customized according to the requirement of the turn ratio. For example, if the turn ratio is $N_p : N_s$ ($N_p < N_s$) when the FML winding is used as a transformer, then, in the first $N_p$ inner turns, the structure of the multilayer foil is the
same as in Fig. 7(a), and in the \( N_p + 1 \) to \( N_s \) turns, it will only have two conductive layers which is the same as in Fig. 6(a). The equivalent circuit is shown in Fig. 7(b) when terminals \( a, c, d, b \) and \( e \) are connected to external circuits. Here \( F2 \) is used to represent this new structure.

Thus, in the modified inverter, FML foils can be employed to integrate the capacitor \( C_t \), the output filter \( L_o \) and the transformer by using the structures \( F1 \) and \( F2 \) in Fig. 6 and Fig. 7, respectively.

As shown in Fig. 8, connections of the combining unit with FML windings and its equivalent circuit are proposed.

In this integrated structure, FML winding \( W2 \) which has the same structure as winding \( F2 \) (i.e., the transformer) is wound at the center leg of the EE core. Two identical FML windings which have same structure as winding \( F1 \) and \( F3 \) in Fig. 8(a), are symmetrically wound at the two outer legs of the ferrite core. Terminals \( d_2 \) and \( e_2 \) of winding \( W2 \) are connected with terminals \( a_1 \) and \( b_1 \) of winding \( W1 \), respectively. Terminals \( c_1 \) and \( d_1 \) of winding \( W1 \) are connected to terminals \( a_3 \) and \( b_3 \) of winding \( W3 \) respectively. The equivalent circuit of this proposed structure is shown in Fig. 8(b) when terminals \( a_2, c_2, b_2, c_3 \) and \( e_2 \) are connected to external circuit. The magnetic characteristic of the combined structure will be explained in detail in the next sub-section.

Then, connect terminals \( a_2, c_2, b_2, c_3 \), and \( e_2 \) of the integrated structure to nodes \( A, B, C, D \), and \( E \) as shown in Fig. 5, respectively, the connections of the FMLF windings in the micro-inverter are presented in Fig. 9.

**2.3 Magnetic Circuit Design**

Assuming the air gaps in two outer core legs are symmetric, the fluxes generated by the inductor current \( i_L \) in winding \( W1 \) and \( W3 \) are shown in Fig. 10 and can be calculated by:

\[
\Phi_{W1} = \Phi_{W3} = N_f \cdot i_L / R_L \tag{1}
\]

where \( N_f \) is the number of turns of \( W1 \) (\( W3 \)), \( R_L \) is the reluctance of the fluxes in \( W1 \) (\( W3 \)).

The fluxes of the winding \( W2 \) (i.e., the transformer) are shown in Fig. 11.

The fluxes \( \Phi_p \) generated by the primary current \( i_p \) and the fluxes \( \Phi_s \), generated by the secondary current in the integrated transformer (i.e., \( W2 \)) as shown in Fig. 11(b) is given by (2).

\[
\Phi_p = N_p \cdot i_p / R_T, \quad \Phi_s = N_s \cdot i_s / R_T \quad \tag{2}
\]

where \( N_p \) is the number of turns of the primary side winding, \( N_s \) is the number of turns of the secondary side winding, \( R_T \) is the reluctance of the fluxes.

As shown in Fig. 12, the total fluxes of the integrated structure are presented. Part of the fluxes generated by winding
W1 in the center core leg is named $\Phi_{T(1)}$. Similarly, the fluxes caused by winding W3 which flow into the center core leg is named $\Phi_{T(2)}$. It can be seen, fluxes $\Phi_{T(1)}$ and $\Phi_{T(2)}$ cancel each other in the center core leg due to the symmetry of winding W1 and W3. Thus, the fluxes generated by these two windings have no influence on the transformer (15). As for the fluxes generated by winding W2, it can be divided into two parts flowing to two outer core legs and named $\Phi_{T(1)}$ and $\Phi_{T(2)}$, respectively. Since the air gaps in two outer leg are identical, the fluxes $\Phi_{T(1)}$ and $\Phi_{T(2)}$ are equal. In the left core leg, $\Phi_{T(1)}$ is opposite to the flux of $\Phi_{T}$, while $\Phi_{T(2)}$ has the same direction as $\Phi_{T}$ in the right core leg. The influence of fluxes $\Phi_{T}$ of W2 will therefore cancel out due to the fact that the inductance of winding W1 and W3 are connected in series. Therefore, the transformer W2 and the inductor $L_p$ (combined W1 and W3) are completely decoupled on the same core (16).

The inductance of the FML winding W1 (W3) is derived as:

$$L_{W1} = L_{W3} = \frac{N_p^2}{R_L} \quad \cdots \cdots \cdots \cdots \cdots (3)$$

The capacitance formed by integrated capacitor of W1 and W3 in the proposed design can be calculated as:

$$C_o = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot l_L \cdot h_L}{t_{DL}} \quad \cdots \cdots \cdots \cdots \cdots (4)$$

where $\varepsilon_0$ and $\varepsilon_r$ are the dielectric constants of the air ($8.85 \times 10^{-12}$) and the dielectric film (2.2), respectively. $l_L$ is the total length of the dielectric film in W1 and W3. $h_L$ and $t_{DL}$ are the height and thickness of the dielectric film, respectively.

As for the integrated transformer, the inductance of the primary side and secondary side can be derived as:

$$L_p = \frac{N_p \cdot \Phi_p}{i_p} = \frac{N_p^2}{R_T} \quad \cdots \cdots \cdots \cdots \cdots (5)$$

$$L_s = n^2 \cdot L_p \quad \cdots \cdots \cdots \cdots \cdots (6)$$

where $1/n$ is the turns ratio (1 : 6 in this paper) of the transformer, i.e. $N_p/N_1$.

The integrated capacitance of winding W2 can be derived with the following formula:

$$C_T = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot l_T \cdot h_T}{t_{DT}} \quad \cdots \cdots \cdots \cdots \cdots (7)$$

where $\varepsilon_0$ and $\varepsilon_r$ are the dielectric constants of the air and the dielectric film. $l_T$ is the total length of the dielectric film in winding W2. $h_T$ and $t_{DT}$ are the height and thickness of the dielectric film, respectively.

2.4 Distributed Component Model

Previous studies had established the distributed component model. The model can be used to verify the characteristic of the FML foils with relatively high accuracy (17). Thus, to better estimate the performance of the proposed design when different terminals are connected, a distributed component model for the integrated FML winding is presented.

The top-view of 2-turn FML foils with typical four-layer structure is presented in Fig. 13(a). The insulation layer is implanted between two consecutive conductive layers. The flying (parasitic) capacitance is thus formed by the 1st conductive layer of the 1st turn and the 2nd conductive layer of the 2nd turn, the distributed capacitance is generated by the dielectric film at the same time as shown in Fig. 13(b).

When the winding is extended to $N$ turns, the equivalent circuit with distributed component model is shown in Fig. 14. For an arbitrarily turn, there are totally four branches which are indicated with numbers in blocks. For example, for the 2nd turn, the numbers are 5, 6, 7 and 8 where branches 5 and 7 are self-inductances, branch 6 is the flying capacitance and branch 8 is the distributed capacitance. This pattern will repeat for each turn expects that the last turn will have another distributed capacitance $C_{kN+1}$. Take the $k^{th}$ turn as an example.

1) Two self-inductances corresponding to two conductive layers and denoted with $L_{1k}$ and $L_{2k}$. 

Test the $k$th turn of the FML winding: 

$$L_{1k} = \frac{N_p^2}{R_{1k}} \quad \cdots \cdots \cdots \cdots \cdots (8)$$

$$L_{2k} = n^2 \cdot L_{1k} \quad \cdots \cdots \cdots \cdots \cdots (9)$$

where $1/n$ is the turns ratio (1 : 6 in this paper) of the transformer, i.e. $N_p/N_1$.
2) The distributed capacitance is

\[ C_{4k} = \frac{C_{1(k-1)} + C_{1k}}{2} \] ........................ (8)

where subscript \( 4k \) indicates the branch number; subscript number 1 indicates FML winding (i.e. W1) and so \( C_{1(k-1)} \) and \( C_{1k} \) indicates the distributed capacitance in the \((k-1)\)th and \(k\)th turn of winding W1, respectively. For the first turn, the distributed capacitance is \( C_4 = C_{11}/2 \); and for the last turn, there will be another distributed capacitance which is \( C_{4N} = C_{1N}/2 \).

3) The flying capacitance is

\[ C_{4k-2} = \frac{C_{1(p(k-1)} + C_{1pk}}{2} \] ........................ (9)

where subscript \( 4k - 2 \) is the branch number; subscript number 1 indicates winding W1; \( C_{1(p(k-1)} \) and \( C_{1pk} \) indicates the flying capacitance created between the \((k-1)\)th and \(k\)th turns and that created between the \(k\)th turn and \((k+1)\)th turns. For the first turn, the flying capacitance is \( C_2 = C_{1p2}/2 \); and for the last turn, it is \( C_{4N-2} = C_{1p(N-1)/2} \).

Besides of the branches, there is mutual inductance between every two self-inductances, which is denoted as \( M_{ij} \) (\( i \) and \( j \) are the branch numbers).

As shown in Fig. 14, the number of independent nodes in the winding with \( N \) turns is \( 2N + 2 \) which are indicated with numbers in ellipses, and the number of branches is \( 4N + 1 \).

The impedance matrix \( Z \) of the \( N \)-turn model can be obtained as (10). All the elements in the impedance matrix \( Z \) can be classified into four kinds: \( Z_{(2i-1)(2j-1)} \) \((i = j = 1, 2, \ldots 2N)\) corresponding to distributed inductance, \( Z_{(4p)(4q)} \) \((p = q = 1, \ldots N)\) corresponding to distributed capacitance, and \( Z_{(4p-2)(4q-2)} \) \((p = q = 1, \ldots N)\) corresponding to flying capacitance, \( Z_{(2i-1)(2j-1)} \) \((i \neq j = 1, 2, \ldots 2N)\) corresponding to mutual inductance. The evaluation of the parasitic capacitance and the distributed capacitance in the model has been investigated in (17).

\[
Z = \begin{bmatrix}
Z_{11} & 0 & Z_{M_{13}} & \cdots & 0 \\
0 & Z_{22} & 0 & \cdots & 0 \\
Z_{M_{13}} & 0 & Z_{33} & \cdots & 0 \\
\cdots & \cdots & \cdots & \cdots & \cdots \\
0 & 0 & 0 & \cdots & Z_{(4N+1)(4N+1)}
\end{bmatrix} \tag{10}
\]

With the equivalent circuit proposed in (3) for the model, the impedance of the source branches should be included in the impedance matrix. Then, the node voltage vector \( V_k \) of the model can be obtained by solving:

\[
(A \cdot Z^{-1} \cdot A^T) \cdot V_k = -A \cdot Z^{-1} \cdot V_{test} \] ........................ (11)

where \( A \) is the incidence matrix of the circuit and \( V_{test} \) is the independent voltage source.

To verify the accuracy of the distributed component model, take a five-turn FML foil with the same structure as the winding W1 as an example. The prototype of the five-turn FML foil is shown in Fig. 15. Any arbitrarily two port can be taken as a T-type equivalent circuit, thus, the test to obtain the characteristic of the FML foil can be divided into three steps: first, terminals \( a \) and \( c \) are connected to the spectrum analyzer E4990A; next, connect terminal \( c \) and terminal \( d \) to the analyzer; then, connect terminal \( a \) and \( d \) together, and connect terminal \( ad \) and \( c \) to the analyzer.

The measured curves are presented in Fig. 16, and the simulation curves derived from the distributed component model are also given.

The impedance curve obtained from the terminals of the FML winding can be solved by:

\[
\begin{align*}
L &= \frac{1}{2 \cdot \pi \cdot f} |Z_{test}| \\
C &= \frac{1}{2 \cdot \pi \cdot f} |Z_{test}| \cdot 2 \cdot \pi \cdot f \tag{12}
\end{align*}
\]

According to the Fig. 16, the FML winding can be used as inductor when terminal \( a \) and \( c \) are connected to circuit, and the inductance is about 570 nH; when terminal \( c \) and terminal \( d \) are connected to outer circuit, the FML winding is equivalent to a capacitor where the capacitance is about 2.0 nF. The winding can be used as a LC parallel circuit when terminal \( ad \) and \( c \) are chosen to connect.
It can be seen that the distributed component model can predict the characteristic of the FML winding with relatively high accuracy, and the results obtained from the experiments further verify that a LC circuit with discrete components can be replaced by a FML foil when terminals a, c, d are connected to outer circuit.

According to connections between the FML winding W2 and winding W1, then, the distributed component model of the secondary side of the transformer and the filter in the integrated design can be obtained as shown in Fig. 17.

3. Design Procedure

The integrated structure is designed based on a 100 W micro-inverter. The expected values of the integrated structure for the inverter are listed in Table 1. To clarify the design procedure, five steps which are explained as follows.

Step 1: Based on the expected values of the transformer and the output inductor, core EE50 is chosen. The core material is DMR95, AL value is 9000 at 25°C.

Step 2: The number of turns of the FML winding W2 and W1 (W3) can be determined by the expected inductances of the transformer and the output filter, the parameters of the ferrite core and the specifications of the inverter as follows:

\[
N_p = \frac{L_p \cdot t_p}{B_{sat} \cdot A_{ec}} \tag{13}
\]

\[
N_f = \frac{L_{W1(W3)} \cdot t_f}{B_{sat} \cdot A_{eo}} \tag{14}
\]

where \(N_p\) is the number of turns of the primary side winding of the transformer (the number of turns of the secondary side winding of the transformer can be obtained according to (6)), \(N_f\) is the number of turns of the winding W1 (W3), \(A_{ec}\) and \(A_{eo}\) are the effective cross-sectional area of the ferrite core of center leg and outer leg, \(B_{sat}\) is the saturated magnetic flux density of the core, which is set to 0.3 T in this paper.

The number of turns of W1 and W3 can be adjusted till the desired value is obtained:

\[
L_{W1} + L_{W3} + 2 \cdot M_{W1(W3)} \approx L_o \tag{15}
\]

Step 3: The maximum width of the conductive layer in W2 and W1 (W3) is restricted according to the dimensions of the ferrite core. Width \(h\) of 35 mm is used for the conductive layers in the proposed design.

The current density \(j_c\) in this paper is set to 5 A/mm² for all conductive layers. Thus, the thickness \(t_c\) of the conductive layer used as the primary side winding of the transformer can be derived as:

\[
t_p = \frac{I_{p,MAX}}{j_c \cdot h} \tag{16}
\]

where \(I_{p,MAX}\) is the maximum current in the primary side of the transformer.

Similarly, a same thickness can be chosen for both the conductive layer of the secondary side winding of the transformer and the filter inductor, since the maximum current \(I_{f,MAX}\) in the filter inductor and the maximum current \(I_{w,MAX}\) in the secondary side winding are at the same level.

\[
t_f = \frac{I_{f,MAX}}{j_c \cdot h} \tag{17}
\]

The total length of the FML windings of W2 and W1 (W3) can be estimated by resolving the formulation below, and the method is introduced in (17).

\[
\begin{align*}
I_p &= 4 \cdot (N_f^2 - N_p) \cdot (p_p + t_p) \\
&+ N_p \cdot (2 \cdot a_{ec} + 2 \cdot b_{ec} + 4 \cdot p_p) + t_f \\
I_f &= 4 \cdot (N_f - N_p) \cdot (N_f - N_p - 1) \cdot (p_f + t_f) \\
&+ (N_f - N_p) \cdot (2 \cdot a_{eo} + 2 \cdot b_{eo} + 4 \cdot p_f) + t_f \\
I_f &= 8 \cdot (N_f^2 - N_p^2) \cdot (p_f + t_f) \\
&+ 2 \cdot N_f (2 \cdot a_{eo} + 2 \cdot b_{eo} + 4 \cdot p_f) + 2 \cdot g_f
\end{align*}
\]

where the \(g_f\) is the clearance between two adjacent turns, \(p_p\) is the thickness of one turn of winding W2 in the first \(N_f\) turns, \(p_f\) is the thickness of one turn of W2 after \(N_f\) turns, and \(p_f\) is thickness of one turn in W1 and W3. \(a_{ec}\) and \(b_{ec}\) is the length and width of the center core leg, \(a_{eo}\) and \(b_{eo}\) is the length and width of the outer core legs, respectively. \(a_{cp}\) and \(b_{cp}\) is the length and width of W2 after \(N_p\) turns are winded. It should be noted that one turn includes two copper layers, one dielectric layer and one insulation layer for W1 and W3 as shown in Fig. 6, while for W2, it includes three copper layers in the first \(N_f\) turns (since \(N_f\) is larger than \(N_p\)), and from \(N_{f+1}\) to \(N_f\) turn, it has the same two conductive foils structure as W1 and W3 do.

The expressions of \(a_{cp}\) and \(b_{cp}\) can be given as:

\[
a_{cp} = a_{ec} + 2 \cdot N_f \cdot (p_f + g_f) \tag{19}
\]

\[
b_{cp} = b_{ec} + 2 \cdot N_f \cdot (p_f + g_f) \tag{20}
\]

Step 4: The integrated capacitance formed by FML winding W1 (W3) and W2 can be calculated with equations (7)
Table 2. Parameters of FML winding

<table>
<thead>
<tr>
<th>Structural Parameters</th>
<th>W2</th>
<th>W1 and W3</th>
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</table>

and (4). Due to the capacitances formed by transformer and output filter are paralleled, the total capacitance \( C_t \) equals to the sum of \( C_o \) and \( C_f \).

The values of the integrated capacitance depend on two factors: the window area of the ferrite core and the material of the dielectric film. In order to obtain the expected capacitance, here, PP film with a thickness 25 μm (\( t_d \)) is chosen as the dielectric layer for the transformer and the output filter.

Step 5: With the four steps above, restrictions of the core window should be satisfied, or another core with bigger dimensions should be used.

The specifications of FMLF winding W2 and W1 (W3) are summarized in Table 2.

4. Experimental Results

The prototype of the proposed structure is constructed, and used in a 100 W micro-inverter to test its performance. The inverter bridge works with line frequency \( f_l \), the switching frequency of \( f_s \) is 50 kHz. In this paper, the input voltage to the inverter is set to around 35 VDC. The RMS voltage of the grid is 230 V. The integrated design is compared with the traditional solution with discrete transformer and output filter. The prototype is shown in Fig. 19. As for the discrete components, the space occupied by the transformer is about 69.6 cm³; the filter inductor is about 51.5 cm³, and the capacitor is about 8.5 cm³. Compared with the discrete passive components, the volume of the integrated structure is reduced by about 15%.

Here, the spectrum analyzer E4990A is used to measure the values of the integrated design. The connections between the analyzer and the FML foils are shown in Fig. 20.

First, terminals \( a_2 \) and \( c_2 \) are connected to the analyzer, and the primary-side inductance of the transformer is obtained as 45.5 μH. Then, terminals \( b_2 \) and \( d_2 \) are connected to the meter and the secondary-side inductance of the transformer is obtained as 1.7 mH. Terminals \( a_1 \) and \( c_1 \) are connected to the analyzer to get the inductance of FML winding W1 which is about 1.1 mH. The inductance of W3 is almost the same. Then, terminals \( d_2 \) and \( e_2 \) of W2 are measured to get
DC voltage, a power resistor of 525 Ω can work properly and output rated power at the given input is 176 nF. The measured curves are shown in Fig. 21. The capacitance integrated in this proposed structure, which includes the discrete output filter and transformer.

Then, the inverter is connected to the grid (230 Vrms, 50 Hz). The experimental waveforms are shown in Fig. 23 and compared with the results of using discrete components.

According to the experimental results, the performance of the integrated structure is almost the same as that of using the discrete output filter and transformer. The temperatures on the core, and winding W1, W2 and W3 of the integrated structure within half an hour after the system is activated at rated power are recorded in Fig. 24. According to the figure, the maximum temperature of the integrated structure is less than 318 K.

5. Conclusion

In this paper, an integrated structure for the transformer and the output filter of a micro-inverter with FMLF technique is proposed. The integrated structure is constructed on an EE core with double-copper foil and triple-copper foil windings. The volume of the proposed structure is reduced by about 15% in comparison with the discrete components. The details of the design process are presented.

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References

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