Experimental Verification of the Large-Current Turn-off of Series-Connected IEGTs for Hybrid DC Circuit Breakers

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This paper considers the application of series-connected press-pack Injection Enhanced Gate Transistors (IEGTs) as semiconductor breakers for hybrid DC circuit breakers (DCCBs) in multi-terminal HVDC transmission systems. In order to interrupt a large current equivalent to a fault current without parallel connection of a press-pack IEGT, a snubber circuit was applied. With the snubber circuit, surge voltages and switching losses can be reduced. In order to balance the voltages across each series-connected IEGT, their characteristics and circuit conditions should be similar, and the operation timings should be adjusted. The performance a prototype hybrid DCCB was evaluated. The semiconductor breaker of the hybrid DCCB prototype was composed of four series-connected IEGTs (4.5 kV, 2.1 kA) with the snubber circuit. The experimental results show that it successfully interrupted a current of 9.5 kA. The peak voltage across the semiconductor breaker was 14.3 kV. The variation in the voltage across each IEGT was less than 5%. This means that the peak voltage of each IEGT was suppressed to less than the withstand voltage of the IEGT.

Keywords: HVDC, Hybrid DCCB, IEGT

1. Introduction

Recently, as one measure to promote the massive introduction of renewable energy, optimization of wide area systems that transmit electric power from large-scale wind power generators located offshore to individual mainland demand areas has been studied. In the case of long-distance transmission, DC transmission is better than AC transmission in terms of losses and construction costs. Therefore, the application of multi-terminal high-voltage DC (HVDC) transmission systems to connect multiple windfarms and multiple onshore stations has been studied. In multi-terminal HVDC transmission systems, in order to prevent fault voltage spreading, large-capacity DC circuit breakers (DCCBs) are required to disconnect fault points in a few milliseconds.

In the past several years, hybrid DCCBs that include mechanical and semiconductor switches have been developed to meet the demands for high-speed interruption. If those hybrid DCCBs have semiconductor devices in the normal current path, the transmission losses in the semiconductor devices will increase.

On the other hand, a low-loss hybrid DCCB has been proposed. The circuit configuration is shown in Fig. 1.

The proposed hybrid DCCB includes mechanical switches, a semiconductor breaker, and a commutation circuit. In the normal mode, the current flows through the mechanical switch. Since there is no semiconductor device in the current path, transmission losses can be minimized. When a fault occurs, the commutation circuit operates and the fault current commutates from the mechanical switch to the semiconductor breaker. Then, the semiconductor breaker can interrupt the fault current.

A press-pack Injection Enhanced Gate Transistor (IEGT) is a semiconductor device suitable for high-voltage/large-current operation. In general use, a press-pack IEGT has the capability to interrupt a current twice as large as the rated current. However, a fault current is assumed to be more than twice as large as the rated current. In order to interrupt a fault current without parallel connection of press-pack IEGTs, the press-pack IEGTs require a current interrupting capability exceeding the normal interruptible current. Furthermore, the press-pack IEGTs need to be connected in series for the purpose of withstanding the high voltages in HVDC transmission systems. The voltages across the series-connected IEGT need to be balanced so as not to exceed the...
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withstand voltage of the IEGTs. However, there are no reports of series-connected IEGTs interrupting a current more than twice as large as their rated current.

For the proposed hybrid DCCB, this paper proposes a configuration that can interrupt a current more than twice as large as the rated current with series-connected IEGTs. To verify the capability of the proposed configuration, a prototype hybrid DCCB that includes a semiconductor breaker with series-connected IEGTs was demonstrated.

2. Basic Operation Principle

The operation process of the proposed hybrid DCCB is as follows (refer to Fig. 2):

(a) A system fault occurs, and the fault current through the mechanical switch increases. (b) When the fault is detected, the disconnector and the breaker start to open. The semiconductor switches of the commutation circuit are turned on. Then, a capacitor in the commutation circuit is discharged, and the current in the breaker decreases. (c) When the current in the breaker falls to zero, the arc of the breaker is extinguished. (d) When the semiconductor breaker is turned on and the semiconductor switches of the commutation circuit are turned off, the fault current commutates to the semiconductor breaker. (e) After insulation recovery of the disconnector, the semiconductor breaker turns off. Then, the fault current commutates to the arrester and decays because the arrester consumes the energy stored in the inductor. Finally, the interrupting operation is completed.

Based on the operation above, we consider the functions of the semiconductor breaker in detail. During normal operation, current does not flow through the semiconductor breaker. Only when a system fault occurs does the fault current flow through the semiconductor breaker and is interrupted by the semiconductor breaker. When the fault current is interrupted, an overvoltage is suppressed by the arrester. In addition to the arrester voltage \( V_{ar} \), the voltage across the stray inductance between the arrester and the semiconductor breaker, \( V_{Ls} \), is applied to the semiconductor breaker.

Figure 3 shows an equivalent circuit diagram and the waveforms of voltage and current of the semiconductor breaker.
The number of semiconductor switches connected in series is determined according to the voltage characteristics of the arrester and the rate of semiconductor switches. In Section 3, in order to describe the operation of snubber circuit simply, semiconductor device is shown of the one series configuration. As shown in Fig. 3, the semiconductor switch of the semiconductor breaker has the function of interrupting a large current equivalent to the fault current. Moreover, it is necessary to suppress the overvoltage so as not to exceed the withstand voltage of the semiconductor breaker.

3. Configuration of the Semiconductor Breaker

Press-pack IEGTs (4.5 kV, 2.1 kA) are used to block high voltage and large current. In general use, a press-pack IEGT has the capability to interrupt a current twice as large as the rated current (4.2 kA). A fault current is assumed to be more than 4.2 kA. Since the fault current flows through the semiconductor breaker for an extremely short time, it is excessive to use many parallel-connected press-pack IEGTs to interrupt the fault current. Instead, we used a snubber circuit to interrupt the fault current without using parallel-connected press-pack IEGTs. Figure 4 shows a circuit diagram in the case where the semiconductor breaker is configured with IEGTs and a snubber circuit. Figure 5 shows the waveforms of voltage and current of the IEGTs with snubber circuit. Applying the snubber circuit makes it possible to suppress the overvoltage, as shown in Fig. 5. In addition, since the current decreases before the voltage rises, it is also possible to suppress the switching losses of the IEGTs. Therefore, the IEGTs can interrupt the fault current safely.

The operation of the IEGTs with the snubber circuit is shown in Figs. 6 and 7 and will be described in detail below.

(Period 1)

When the IEGTs start to turn off, the IEGT voltages begin to rise, and at the same time, the snubber circuit current $I_s$ starts to charge the snubber capacitor $C_s$, and the voltage across the snubber capacitor starts to rise. As $I_s$ increases, the IEGT current $I_{ce}$ decreases. Since there is a stray inductance $L_{snb}$ between the snubber circuit and the IEGTs, the voltage across the IEGTs, $V_{ce}$, becomes higher than the voltage across the snubber capacitor due to the voltage across $L_{snb}$. In this period, $V_{ce}$ is approximated by:

$$V_{ce} = L_{snb} \frac{dI_s}{dt} + \int_0^t \frac{I_s}{C_s} dt.$$  \(\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\quad\-quarters of \text{ a } \text{ series } \text{ resonant } \text{ circuit } \text{ of } L_s, \text{ } L_{snb} \text{ and } C_s \text{ is formed. The maximum}
value of the surge voltage $\Delta V_p$ across the series circuit of $L_s$ and $L_{snb}$ and the maximum value of the surge voltage $\Delta V_{cep}$ across the IEGTs satisfy the following relationships:

\[ I_{brk}^2 (L_s + L_{snb}) = \Delta V_p^2 \cdot C_s. \quad \cdots \cdots \cdots \cdots \cdots \cdots \cdots (4) \]

\[ \Delta V_{cep} = \Delta V_p \cdot \frac{L_s}{L_s + L_{snb}}. \quad \cdots \cdots \cdots \cdots \cdots \cdots \cdots (5) \]

Simplifying Eq. (4) and Eq. (5) yields:

\[ \Delta V_{cep} = I_{brk} \sqrt{\frac{L_s}{C_s (L_s + L_{snb})}}. \quad \cdots \cdots \cdots \cdots \cdots \cdots \cdots (6) \]

Therefore, the peak voltage of the IEGTs, $V_{cep}$, is given by:

\[ V_{cep} = V_{ar_res} + I_{brk} \sqrt{\frac{L_s}{C_s (L_s + L_{snb})}}. \quad \cdots \cdots \cdots \cdots \cdots \cdots \cdots (7) \]

As shown in (6), $L_s$ and $L_{snb}$ affect $\Delta V_{cep}$.

$V_{cep}$ can be suppressed to below the withstand voltage of the IEGTs by proper selection of $C_s$. Since the duration of Period 3, $T_3$, is $\frac{1}{4}$ of the period corresponding to the resonant frequency, $T_3$ is given by:

\[ T_3 = \frac{\pi}{2} \cdot \sqrt{\frac{L_s + L_{snb}}{C_s}}. \quad \cdots \cdots \cdots \cdots \cdots \cdots \cdots (8) \]

When the whole current commutates to the arrester, the turn-off operation of the IEGTs and the snubber circuit is completed.

Also in this period, since current does not flow in the IEGTs, losses do not occur in the IEGTs.

Considering the above, we compare switching losses of the IEGTs and the surge voltage across the IEGTs for cases with a snubber circuit and without a snubber circuit. For simplicity, the comparison is made with a model assuming that $dV_{cep}/dt$ without the snubber circuit is a constant value $\alpha$ and $dI_c/dt$ values without the snubber circuit and with the snubber circuit are equal and constant value $-\beta$.

In the case without the snubber circuit, the voltage across the IEGTs, $V_{cep}$, and the IEGT current, $I_c$, satisfy the following relationships:

\[ V_{cep} = \begin{cases} \alpha \cdot t & \text{Period0} \\ V_{ar_res} + L_s \cdot \frac{dI_c}{dt} & \text{Period1} \end{cases} \quad \cdots \cdots \cdots \cdots \cdots \cdots \cdots (9) \]

\[ I_c = \begin{cases} I_{brk} & \text{Period0} \\ I_{brk} - \beta \cdot t & \text{Period1} \end{cases} \quad \cdots \cdots \cdots \cdots \cdots \cdots \cdots (10) \]

The surge voltage across the IEGTs without the snubber circuit, $\Delta V_{cep, wos}$, is given by:
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\[ \Delta V_{\text{cep\_wos}} = I_s \cdot \beta \] \hspace{1cm} (11)

Since the duration of Period 0, \( T_0 \), is the time until \( V_{\text{ce}} \) rises from 0 to \( V_{\text{ar\_res}} \), \( T_0 \) is given by:

\[ T_0 = \frac{V_{\text{ar\_res}}}{\alpha} \] \hspace{1cm} (12)

Therefore, the switching loss of the IEGTs during Period 0, \( E_{\text{wos\_0}} \), is given by:

\[ E_{\text{wos\_0}} = \int_0^{T_0} I_{\text{brk}} \cdot \alpha \cdot t \cdot dt \]
\[ = \frac{1}{2} \left( \frac{I_{\text{brk}} \cdot \alpha \cdot I_{\text{brk}} \cdot V_{\text{ar\_res}}}{\alpha} \right) \]
\[ = \frac{I_{\text{brk}} \cdot V_{\text{ar\_res}}}{2} \] \hspace{1cm} (13)

Since the duration of Period 1, \( T_1 \), is the time until \( I_c \) decreases from \( I_{\text{brk}} \) to 0, \( T_1 \) is given by:

\[ T_1 = \frac{I_{\text{brk}}}{\beta} \] \hspace{1cm} (14)

Therefore, the switching loss of the IEGTs during Period 1, \( E_{\text{wos\_1}} \), is given by:

\[ E_{\text{wos\_1}} = \int_0^{T_1} (I_{\text{brk}} - \beta \cdot t) \cdot (V_{\text{ar\_res}} + L_s \cdot \beta) dt \]
\[ = \frac{I_{\text{brk}}^2 \cdot V_{\text{ar\_res}}}{2 \beta} + \frac{L_s \cdot I_{\text{brk}}^2}{2} \] \hspace{1cm} (15)

From Eqs. (13) and (15), the total switching loss of the IEGTs without the snubber circuit, \( E_{\text{wos}} \), is given by:

\[ E_{\text{wos}} = \frac{I_{\text{brk}} \cdot V_{\text{ar\_res}}}{2 \cdot \alpha} + \frac{I_{\text{brk}}^2 \cdot V_{\text{ar\_res}}}{2 \cdot \beta} + \frac{L_s \cdot I_{\text{brk}}^2}{2} \] \hspace{1cm} (16)

In the case with the snubber circuit, loss occurs only during Period 1. Considering \( I_c = \beta \cdot t \), the voltage across the IEGTs, \( V_{\text{ce}} \), and the IEGT current, \( I_c \), satisfy the following relationships:

\[ V_{\text{ce}} = L_{\text{sub}} \beta + \int_0^{t} \frac{\beta \cdot t}{C_s} dt = L_{\text{sub}} \beta + \frac{\beta}{2 \cdot C_s} \cdot t^2 \] \hspace{1cm} (17)

\[ I_c = I_{\text{brk}} - \beta \cdot t \] \hspace{1cm} (18)

The surge voltage across the IEGTs with the snubber circuit, \( \Delta V_{\text{cep\_s}} \), is equal to \( \Delta V_{\text{cep}} \) in Eq. (5). Therefore, the total switching loss of the IEGTs with the snubber circuit, \( E_s \), is given by:

\[ E_s = \int_0^{I_{\text{brk}}} (I_{\text{brk}} - \beta \cdot t) \left( L_{\text{sub}} \beta + \frac{\beta}{2 \cdot C_s} \cdot t^2 \right) dt \]
\[ = \frac{I_{\text{brk}}^2 \cdot L_{\text{sub}}}{2} + \frac{I_{\text{brk}}^4}{24 \cdot C_s \cdot \beta^2} \] \hspace{1cm} (19)

Assuming that the conditions in Table 1 are used, \( E_{\text{wos}} = 175 \) [J] and \( E_s = 52 \) [J]. Therefore, the total switching loss of the IEGTs with the snubber circuit, \( E_s \), can be reduced to about 30% of that without the snubber circuit, \( E_{\text{wos}} \). Then \( \Delta V_{\text{cep\_wos}} = 5.0 \text{kV} \) and \( \Delta V_{\text{cep\_s}} = 2.2 \text{kV} \). Therefore, the surge voltage across the IEGTs with the snubber circuit, \( \Delta V_{\text{cep\_s}} \), can be reduced to about 45% of that without the snubber, \( \Delta V_{\text{cep\_wos}} \).

From the above operation, it is possible to suppress an overvoltage in the IEGTs and losses with the snubber circuit.

Furthermore, in order to withstand a high voltage equivalent to those in HVDC systems, the semiconductor breaker is constituted of series-connected IEGTs. In order to suppress the voltage across each IEGT to less than the withstand voltage across the IEGT, voltage balancing of each series-connected IEGT is required. As mentioned in the reference (10), the voltage imbalance is less when \( dV_{\text{ce}}/dt \) is small; because the voltage imbalance with respect to the timing deviation becomes small. Since \( dV_{\text{ce}}/dt \) is suppressed with the snubber circuit, the installation of the snubber circuit contributes to the voltage balance. The voltage balance is also mainly influenced by the characteristics of each IEGT, the circuit conditions and the driving speed. In order to balance the voltage across each series-connected IEGT, we made the characteristics of each IEGT and the circuit conditions of

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Table 1. Values of parameters in the comparison for cases with the snubber circuit and without the snubber circuit

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Residual voltage of the arrester</td>
<td>( V_{\text{w_eo}} )</td>
<td>10 kV</td>
</tr>
<tr>
<td>Breaking current</td>
<td>( I_{\text{brk}} )</td>
<td>10 kA</td>
</tr>
<tr>
<td>Steady inductance between the arrester and IEGTs</td>
<td>( L_s )</td>
<td>1 \muH</td>
</tr>
<tr>
<td>Steady inductance between the snubber circuit and IEGTs</td>
<td>( L_{\text{sub}} )</td>
<td>1 \muH</td>
</tr>
<tr>
<td>Snubber capacitance</td>
<td>( C_s )</td>
<td>10 \muF</td>
</tr>
<tr>
<td>IEGTs voltage change rate</td>
<td>( \alpha )</td>
<td>20 kV/\muA</td>
</tr>
<tr>
<td>IEGTs current change rate</td>
<td>( \beta )</td>
<td>5 kV/\muA</td>
</tr>
</tbody>
</table>

\[ E_{\text{wos}} = \frac{I_{\text{brk}} \cdot V_{\text{ar\_res}}}{2 \cdot \alpha} + \frac{I_{\text{brk}}^2 \cdot V_{\text{ar\_res}}}{2 \cdot \beta} + \frac{L_s \cdot I_{\text{brk}}^2}{2} \]
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4. Experimental Results

We built and tested a prototype of the proposed hybrid DCCB and evaluated the behavior of the semiconductor breaker. The circuit diagram of the prototype semiconductor breaker is shown in Fig. 9. The semiconductor breaker was composed of four series-connected IEGTs (4.5 kV, 2.1 kA) with a snubber circuit.

Figure 10 shows the turn-off waveforms of the semiconductor breaker in the experiment of the prototype of the proposed hybrid DCCB. The semiconductor breaker with the series-connected IEGTs and the snubber circuit successfully interrupted a large current of 9.5 kA, and the peak voltage across the semiconductor breaker was 14.3 kV. In this experiment, \( V_{\text{ar}} = 10 \text{kV} \) and \( L_s \sqrt{C_s (L_s + L_{\text{snb}})} = 0.45 \). Substituting these values into Eq. (7) gives \( V_{\text{cep}} = 14.3 \text{kV} \), which is in good agreement with the experimental results.

The waveforms show that the current decreased before the voltage rose. Therefore, and switching losses of the IEGTs were suppressed. Figure 11 shows the peak voltage across the IEGTs in the experiment. The result demonstrated that the variation in the peak voltage of each IEGT was less than 5%, and the peak voltage of each IEGT was suppressed to less than the withstand voltage of the IEGT. As shown in Fig. 10, it is considered that \( \frac{dV_{\text{cep}}}{dt} \) is suppressed by application of the snubber circuit, which contributes to the voltage balance.

5. Conclusion

This paper presented a semiconductor breaker for the proposed hybrid DCCB. Series-connected IEGTs with snubber circuits were applied. Experimental results obtained with the prototype hybrid DCCB showed that it successfully interrupted a high voltage and large current. Moreover, it was confirmed that the voltage balance of each series-connected IEGT was adequate.

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