A Charge Balanced C-V Converter for a Differential Capacitance Sensor

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This paper presents a simple new configuration for a switched capacitor type C-V converter based on a charge balance principle for a differential capacitance sensor and its simulation results. The new converter was devised and realized using only one operational amplifier, nine CMOS switches and an oscillation circuit. It was shown that the offset output due to the input offset voltage of an operational amplifier can be ideally reduced to zero with an appropriate additional switch configuration.

By using a P-Spice circuit simulator, the offset cancellation scheme and proper transient response were confirmed for possible parasitic capacitances concerned in a typical differential capacitance sensor. In addition, a P-Spice system simulation based on analog behavioral models enabled us to reliably estimate the operation of an electro-mechanical system with the C-V converter statically and dynamically, where the electrostatic force acting on a movable electrode was taken into account.

Keywords: Capacitive sensor, C-V converter, P-Spice simulation, Switched capacitor circuit

1. Introduction

A differential capacitance sensing scheme is preferred for various capacitive micro-mechanical sensor systems such as pressure, acceleration, and angular rotation sensors because of its superior common mode signal rejection capability. Figure 1 shows an example of an equivalent circuit for a differential capacitance sensor with four terminal electrodes, where C₁ and C₂ are the sense capacitances, and the capacitances denoted as C_{sx} and C_{px}, where x = 1,2,3,13, are stray capacitances, which should be taken into account in a real microstructure for a proper estimation of the sensor function. On the other hand, C_{s1} and C_{s2} are stray capacitances, which in principle cannot be separated from C₁ and C₂, therefore their capacitance values should be kept as small as possible in order not to degrade the sensitivity and the linearity of the sensor.

To detect the accurate displacement of a mechanically movable microelectrode from the differential capacitance change, one needs to consider a C-V converter, which is immune to the stray capacitance C_{px} and input capacitance C_{in} of the amplifier in order to maintain proper sensitivity as well as the linearity and the dynamic stability of the output. Furthermore, the electrostatic net force between the electrodes due to the AC drive voltages of the detection circuit should be minimized especially for a microsensor with a small spacing between each electrode, otherwise, the movable electrode will stick to the fixed one, resulting in a total failure of the sensor function in some extreme cases. In addition, the electrostatic force will cause an output non-linearity problem, because the force attracts the movable electrode.

There have been several detection methods introduced and applied to capacitive sensors\(^{(1)}\)\textsuperscript{—(7)}. For example, the capacitance AC bridge based on the well-known concept of transformer-ratio-arm bridge\(^{(1)}\textsuperscript{(8)}\) in principle, has an output proportional to the displacement, however, it is not immune to C\(_{in}\) and C\(_{p2}\). It also needs a large load resistance to stabilize the DC offset, occupying a large die area for the circuit. In addition, the complementary drive voltages applied to the fixed electrodes generate a net electrostatic force, which depends on the stray capacitances.

On the other hand, a CMOS compatible readout circuit using a switched-capacitor technique by Cho and Wise\(^{(2)}\textsuperscript{(3)}\) is immune to stray capacitances C\(_{in}\) and C\(_{p2}\). However the net electrostatic force and non-linearity of the output with respect to the displacement should be carefully dealt with in the design of the microsensor accompanying the circuit.

A self-balancing capacitor bridge also based on the charge/discharge method devised by Leuthold is an ideal circuit in terms of the aspects described above, however, in principle, this circuit has an offset voltage from the input offset voltages of the operational amplifiers, whose temperature drift will be a problem for accurate displacement detection in a wide range of operational temperatures. With the charge/discharge methods referred to above, a careful design also should take into account the charge injection of the CMOS switches, nevertheless the feedthrough charges from a switch will generate an other offset, thus also

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Fig. 1. Differential capacitance and associated stray capacitances.
In the following sections, we describe a method of minimizing the offset errors, and the static and dynamic response on the modified self-balancing (charge balanced) circuit consisting of reduced active and passive electrical elements compared to a circuit already reported\(^3\). Results, which confirm the offset reduction and dynamic stability of the circuit by P-Spice circuit simulation will also be discussed where possible stray capacitances are considered. In addition, a system level simulation of a mechanical sensor element and the detection circuitry was carried out to confirm proper sensor system functioning, where the electrostatic force between the movable and fixed electrodes, and displacement to capacitance conversion were considered.

2. Charge Balanced C-V Converter

\subsection{2.1 Basic Principle and Offset Error Cancellation}

Neglecting \(C_{px}\), in Fig. 1, if the sensor element contains two sense capacitances \(C_1\) and \(C_2\), which differentially shift their value upon an applied sense signal and also contains parallel stray capacitances \(C_{s1}\) and \(C_{s2}\), the electrical potential \(V_o\) of the movable electrode when \(V_s\) is supplied to the A-pad and the B-pad is grounded, is simply expressed as follows,

\[V_o = \frac{C_s + C_{s1}}{C_1 + C_{s1} + C_2 + C_{s2}} V_s\]

\[= \frac{1}{2} \left[ 1 + \left( \frac{C_1 + C_2 + C_{s1} + C_{s2}}{C_1 + C_2 + C_{s1} + C_{s2}} \right) \right] V_s \]

where \(C_1\) and \(C_2\) are the sense capacitances ideally defined as follows.

\[C_i = \frac{C_s}{1 - \frac{x}{g_0}} C_i = \frac{1}{1 + \frac{x}{g_0}} \quad (i = 1, 2) \]  

where \(C_s\) is the initial capacitance assuming \(C_1\) and \(C_2\) are equal to each other when the displacement of the movable electrode \(x = 0\), and \(g_0\) the initial spacing between the fixed electrodes and the movable electrode. If \(C_{s1}\) and \(C_{s2}\) are neglected, Equation (1) can be re-written simply using Equation (2) as follows.

[Diagram]

\[V_o = \left(1 + \frac{x}{g_0}\right) \frac{V_s}{2} \]  

By measuring \(V_o\), therefore, a voltage which is completely linear to the displacement \(x\) of the movable electrode can be obtained and the original sensitivity of \(V_o/2g_0\) per unit displacement can be maintained. However, in reality, as shown in Fig. 1, due to the stray capacitances \(C_{s1}\) and \(C_{s2}\) of the sensing element and \(C_{s2}\) of a detection circuit, the sensitivity and the linearity will be degraded depending on the electrical connection of the element and the circuit type. To detect the electrical potential \(V_o\) of the sense port having an extremely high output impedance (C-pad) from DC, and to keep the original characteristic as much as possible, a charge-balanced C-V converter based on a switched-capacitor technique shown in Fig. 2 can be adopted. The figure shows the configuration of the charge balanced circuit for a differential capacitance sensor with an offset compensation scheme regarding the input offset voltage of the operational amplifier, where the circuit employs nine CMOS analog switches, two internal capacitances acting as a feedback capacitance \(C_1\) and as a sample-hold capacitance \(C_2\), and single operational amplifier. There are no external electrical elements needed for this circuit. The switches are driven by the non-overlapping clock phases shown in Fig. 2(b). Here, \(V_s\) and \(V_o\) are the supply voltage and the reference voltage respectively.

When switch \(S_1\) is on (sampling mode), the charge stored in \(C_1\) is released, and charges \(Q_1\) and \(Q_2\) will be stored in capacitors \(C_1\) and \(C_2\) respectively, depending on the voltage \(V_{in}\) updated in every holding mode. If there is the charge difference \(\Delta Q = Q_1 - Q_2\) then in the next phase when \(S_2\) is on (holding mode), the voltage \(V_{in}\) will be increased or decreased depending on the sign of the charge difference during the On period of \(S_1\). This voltage \(V_{in}\) will converge to the value expressed by Equation (3), at which the same charge \((\Delta Q = \Delta Q)\) will be stored in each capacitor balancing the net electrostatic forces between the electrodes. Therefore, a big advantage of this circuit is an immunity to the sensitivity to the stray capacitances \(C_{s1}\) and \(C_{s2}\) shown in Fig. 1. This is due to the fact that the clock drives the objective terminals (A-pad and B-pad) of \(C_1\) and \(C_2\), and only the following charge difference at C-pad is detected. The other stray capacitances such as \(C_{s3}\), \(C_{p3}\), and \(C_{p13}\) have also in principle no effect on the operation of the circuit.

In a real situation when using the operational amplifier shown in Fig. 2, however, the voltage \(V_{in}\) held at capacitor \(C_2\) is not equal to the voltage at C-pad, having a voltage difference defined as \(V_{in}\) between each input offset voltage. The condition of convergence in this circuit when considering \(V_{in}\) is as follows,

\[Q_2 - Q_1 = V_{in} \left( C_1 + C_2 + C_{s1} \right) \]

This relation results in the voltage \(V_{in}\) with an offset error \(V_{off}\), which is expressed as follows,

\[V_{in} = \frac{C_1}{C_1 + C_2} V_s + V_{off}, \quad V_{off} = \frac{C_1}{C_1 + C_2} V_{in} \]

Since for a microsensor \(C_1\) and \(C_2\) are typically 1 pF or less, and \(C_3\) should be somewhat larger than these values to stabilize this circuit as described later, the coefficient \(C_1/(C_1+C_2)\) will be much larger than unity, and the effect of input referred offset voltage \(V_{in}\)
being typically $\pm 20\text{mV}$ for MOS op amps having a temperature dependence\(^{(9)}\) will be amplified, resulting in a large $V_{\text{off}}$ error.

To overcome this disadvantage, the offset cancellation scheme can be implemented as shown in Fig. 2 (for a circuit without this cancellation scheme, switch $S_{1A}$ is removed, and $S_{2A}$ is shortened). Referring to Equations (4) and (5), apparently the term, $C_1 V_{\text{off}}$, contributes to a large offset error $V_{\text{off}}$. This charge, however, can be cancelled by way of pre-charging $C_1$ with $V_{\text{in}}$ when switch $S_{1A}$ is on ($Q_4 = V_{\text{in}} C_4$), and the condition of convergence will be rewritten as Equation (6), ideally eliminating the $V_{\text{off}}$ error.

\[
Q_1 - Q_1 + Q_3 = V_{\text{in}} \left( \frac{C_1 + C_2 + C_3}{C_1} \right) \quad \ldots \ldots \ldots \ldots (6)
\]

\[
V_{\text{in}} = \frac{C_1}{C_1 + C_2} V_{\text{os}} \quad \ldots \ldots \ldots \ldots (7)
\]

On the other hand, there is another output offset caused by the inherent charge injection error from a CMOS switch when it is turning off. This error can be minimized through adopting a dummy switch configuration by which the feed-through charge can be drastically reduced\(^{(9)}\).

### 2.2 Transient response
Neglecting the effect of $V_{\text{off}}$ for the simplicity of the analysis, during the holding sequence $j$, the voltage change $\Delta V_{\text{in}}$ is given by

\[
\Delta V_{\text{in}} = V_{\text{in}}(j) - V_{\text{in}}(j-1) = V_{\text{C}} \left( \frac{V_{\text{in}}(j) + V_{\text{in}}(j-1)}{C_1 + C_2 + C_3} \right) \frac{E}{2 f_{\text{s}}} \quad \ldots \ldots \ldots \ldots (8)
\]

where $E$ is defined as a time derivative of the amplifier output when $\Delta V_{\text{in}} = V_+ - V_-$ is applied between the input terminals of the amplifier, and $f_s$ is the sampling frequency defined in Fig. 2(b). Defining $X$ as the normalized displacement ($X(g_0)$), the transfer function of this circuit $G(z)$ is expressed using a $z$-transformation, corresponding to a first-order electro-mechanical system as follows

\[
G(z) = \frac{Y(z)}{X(z)} = \frac{EB}{4 f_s} \frac{z}{z^2 - 1 - \frac{EB}{2 f_s}} \quad \ldots \ldots \ldots \ldots (9)
\]

\[
B = \frac{C_1 + C_2}{C_1 + C_2 + C_3} \quad \ldots \ldots \ldots \ldots (10)
\]

This system will be stable when the following condition is satisfied,

\[
\frac{1}{4 + \frac{2C_1}{C_0} \left( 1 - X^2 \right) f_s} E < 1 \quad \ldots \ldots \ldots \ldots (11)
\]

The cut-off frequency of this circuit is approximately expressed as follows,

\[
f_s \approx \frac{EB}{4 \pi} \quad \ldots \ldots \ldots \ldots (11)
\]

In the design of this circuit, referring to Equations (10) and (11), one needs to select the proper values for $C_1 / C_{\text{os}}$, the sampling frequency $f_s$, and $E$ in terms of the system stability and response. As for the $E$ value in a real operational amplifier, it is non-linear to the voltage difference between the positive and negative input terminal ($V_+ - V_-$) as shown in Fig. 3 when a commercially available FET input OP Amp (AD820) is used as an example. In the following section, the P-Spice circuit simulation results are described in terms of the offset reduction and the transient response where input offset $V_{\text{in}}$, the non-linear $E$ value can be considered for precise output estimation.

### 3. P-SpICE Simulation
The charge-balanced C-V converter shown in Fig. 2 was simulated using P-Spice in order to confirm the offset cancellation scheme and the dynamic stability of the circuit. Figure 4 shows an example of a full system model for a typical electro-mechanical system including the C-V converter block (4a, 4b), a mechanical element block (4d), an electrostatic simulation block (4c), and a displacement to capacitance converter block (4e). In the case of the offset and its transient simulation, to see the effect of the capacitance $C_3$, only the charge balanced C-V converter block shown in Fig. 4a was used.

#### 3.1 Offset output $V_{\text{off}}$

The simulation was carried out with and without the offset cancellation scheme described in the previous section. The results are shown in Fig. 5. The conditions set in the simulation were $C_1 = C_2 = 1 \text{pF}$, $f_s = 250 \text{KHz}$, $C_3 = 100 \text{pF}$, and $V_{\text{in}} = 5 \text{V}$ with two parameter cases of $C_1 = 300 \text{pF}$ and $500 \text{pF}$. The equal capacitances $C_1$ and $C_2$ were placed between A-pad and C-pad, and between B-pad and C-pad respectively. All possible stray capacitances were set to zero. With these conditions the output of the circuit should ideally be 2.5 V. As shown in Fig. 5, the cancellation scheme employed in Fig. 2 is quite effective in the reduction of the offset shift, being 0.8 mV and 1.3 mV for $C_3 = 300 \text{pF}$ and $500 \text{pF}$ respectively which are extremely small compared to 21 mV and 34 mV corresponding to the values defined by Equation (5) when $V_{\text{in}}$ of AD820 is 140 $\mu \text{V}$.

#### 3.2 Transient Response
Transient responses were simulated on the same circuit with the offset cancellation scheme with the parameters ranging from $C_1 = 20 \text{pF}$ to $200 \text{pF}$, and typical results are shown in Fig. 6. The cutoff frequency of each case is provided with Equation (11) implying a rapid response with a smaller $C_3$. A rough estimation of the minimum value of $C_1$ as the response stability limit predicted by Equation (10) is 25 pF when $E$ equals a constant value of $1.35 \times 10^7 \text{V/sec}$. In the simulation result, however, the circuit is still stable when $C_1 = 20 \text{pF}$ because of the fact of the nonlinear relation of $E$ vs. $V_+ - V_-$. In addition, if the sampling $f_s$ is doubled, the system has a more stable response as seen in the cases with a smaller capacitance.
value of $C_3 = 20 \text{ pF}$. Based on these results and considerations, a sampling frequency $f_s$ as high as realistically possible and a proper capacitance ratio $C_1/C_0$ can be selected in terms of the system response and the stability requirement.

### 3.3 Stray Capacitance Effect

The effect of stray capacitance $C_{p2}$ on the sensitivity defined in Equation (3) was examined in the same circuit with $C_1 = 1.25 \text{ pF}$ and $C_2 = 0.833 \text{ pF}$, which corresponds to the case of the normalized displacement $X = 0.2$. With these capacitance values, the output $V_{\text{out}}$ ideally should be 3.0 V. The result is shown in Fig. 7 with $C_{p2}$ ranging from 0 pF to 10 pF in 5 pF steps, giving extremely large stray capacitances, where the terminal D-pad was grounded. As seen in the figure, the effect on the sensitivity from the stray capacitance was really small as can be understood from the circuit principle explained. The transient response was affected a little depending on $C_{p2}$. The effect on the sensitivity from possible stray capacitances of $C_{p1}$, $C_{p2}$, $C_{p3}$, and $C_{p13}$ of being up to 1.5 pF were less than 1%.

### 3.4 System model simulation

To see and check the effect of the net electrostatic force generated by the circuit on a mechanical sensor element, we need to simulate the total electro-mechanical system with a micro-accelerometer element, and the readout circuit. We constructed a system model by using the P-Spice analog behavioral models shown in Fig. 4. In the mechanical element block (d) of the figure, the mechanical second order system is based on two integrators with two respective feedback forces, one is a spring force and the other is a damping force. The mechanical displacement $x$ and the electrostatic force $F_{\text{es}}$ are governed by the following two equations.

$$x[s^2 + (\omega_n/Q)s + \omega_n^2] = A + F_{\text{es}}/M \quad \text{equation (12)}$$

![Fig. 4. A P-Spice schematics for the electro-mechanical system.](image)

![Fig. 5. Offset output $V_{\text{out}}$ of the circuit with and without the cancellation scheme.](image)

$$F_{\text{es}} = \frac{S_{\text{ele}}}{2} \left[ \frac{(V_{\text{g}} - V_{\text{a}})^2}{(g_{\text{p}} + x)^2} - \frac{(V_{\text{g}})^2}{(g_{\text{p}} + x)^2} \right] \quad \text{equation (13)}$$

where $s$ is the Laplace operator, $\omega_n$ the resonant angular velocity, $Q$ the quality factor, $A$ the Acceleration, $M$ the seismic mass, $F_{\text{es}}$ the electrostatic force, $g_{\text{p}}$ the initial electrode gap, $S$ the electrode surface area and $\varepsilon$ the electric permittivity of a vacuum. In the electrostatic force calculation block (c) in Fig. 7, the force is simulated according to Equation (13). Based on the output displacement $x$ of the mechanical element, the differential capacitances are generated according to the formula stated in Equation (2) through two EVALUATE elements and YX V variable admittance elements with each initial capacitance defined as $C_{10}$.
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These capacitance changes are reflected on the charge balanced C-V Converter to simulate the electrical output of the system. To compare the advantages of the charge balanced C-V Converter with a conventional converter based on the charge difference \( C_1 - C_2 \), the circuit for a differential capacitance sensor shown in Fig. 4b was used. When neglecting the stray capacitances \( C_{s1} \) and \( C_{s2} \), the output signal \( V_{out} \) based on the charge difference is as follows,

\[
V_{out} = \left( 1 + \frac{(C_1 - C_2)}{C_f} \right) V_g + \frac{1}{2} \frac{2C_{x/g_o}}{C_f(1-x/g_o)} V_s \quad \text{(14)}
\]

Figure 8 shows the transient simulation results of the normalized displacement \( \frac{x}{g_o} \) of the movable mass and the electrical output signal \( V_{out} \) of the converter when step accelerations of 4G and 8G were initiated at 0.2 ms with simulation conditions of \( \omega_n = 4430 \text{ rad/sec}, \; Q=0.707, \; \varepsilon = 8.85 \times 10^{-12} \text{ F/m}, \; g_o = 5 \times 10^{-6} \text{ m}, \; \text{ and } S=5.65 \times 10^{-3} \text{ m}^2 \).

Figure 9 shows the linearity of the displacement and the output. In the simulations, possible stray capacitances \( C_{ps} = 1 \text{ pF}, \; C_{ua} = 2.5 \text{ pF} \) (AD820) were also included. The ideal \( \frac{x}{g_o} \) should be 0.4 and 0.8, and the ideal output \( V_{out} \) should be 3.5 V and 4.5 V for the respective accelerations 4G and 8G. When using the charge balanced C-V converter, even when the displacement \( \frac{x}{g_o} \) exceeds 0.8, a mechanically stable and linear response of the movable electrode and the corresponding electrical linear output \( V_{out} \) can be obtained as shown in Fig. 8 and Fig. 9. The linearity of the output was less than 0.05% (8G FS.) in this simulation.

On the other hand, when using the charge difference C-V converter, the system was unstable and the movable electrode stuck to the fixed upper electrode when the acceleration exceeded 4G, because of the unbalanced electrostatic force always generated when the movable electrode was displaced once. In addition to the intrinsic output non-linearity of the circuit in terms of the displacement (Eq.(14)), a large non-linearity (6.4%) of the displacement \( \Delta V \) due to the unbalanced electrostatic force can also be observed for the full scale acceleration of 4G.

4. Conclusions

A charge balanced C-V converter with a low offset drift and a simple circuit configuration was realized and verified through a
system level P-Spice simulation with possible stray capacitances considered. This circuit is quite suitable for a micro-mechanical capacitive sensor with small electrode spacings between movable and fixed electrodes, since it can be operated over a wide range of normalized displacement without an electrostatic stiction problem caused by the electrostatic force and without degrading the output linearity, and it is mostly immune to possible stray capacitances of the sensor element and the detection circuit, thus having a long-term reliability of the sensor output. The system level simulation used for the design of this circuit can be applied to examine system responses where electrostatic actuations for mechanical elements are involved.

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References

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