High-efficient Chip to Wafer Self-alignment and Bonding for Flexible and Size-free MEMS-IC Integration

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Keywords: size-free integration, self-alignment, SAM, lift-off, plasma activated bonding, MEMS

The large-scale and low-cost integration of various MEMS devices with ICs is significantly important for MEMS ubiquitous applications and commercialization. Especially in recent years, the application of wireless sensor network in green manufacture, environmental monitor, and life innovation etc. requires various types of integrated MEMS sensor nodes with different functions, compact-size and extremely low power consumption, to which the flexible integration of MEMS devices with signal processing and wireless data transmission ICs is believed the most promising solution for the pursuit of better device performance as well as to reduce the cost.

Although MEMS-IC integration has been well studied both in academy and in industry for many years, it still needs our great efforts to improve the process flexibility and to reduce the cost. Therefore, in this paper, a two-step process by using carrier wafer was proposed for MEMS-IC flexible and size-free integration. Fig. 1 shows the details process flow.

In the first step, MEMS or IC KGDs with various sizes are picked up from different MEMS or IC processed wafers, aligned to binding-sites on carrier wafer, and then temporarily bonded onto binding-sites. The C2W rapid alignment is one of the key techniques to be developed, since robot alignment occupies tens of seconds or even minutes for each chip. In this work, hydrophobic self-assembled monolayer (SAM) was successfully patterned by lift-off process to define the binding-sites on hydrophilic surface of the SiO2 carrier wafer, and then KGDs could be self-aligned to binding-sites with high speed (in milliseconds) and high accuracy (<1 µm) by capillary force of H2O (as shown in Fig. 2). Compared with other self-alignment and surface treatment processes, this method offers unique and attractive advantageous of simple process and low-cost.

In the second step, those KGDs were transferred from carrier wafer to target IC wafer or interposer wafer by permanent bonding. Au thin film is used as bonding pads and for electric inter-connection as well. Ar plasma treatment was applied to Au film prior to bonding for surface activation, which was proved effective to reduce the bonding temperature to below 200°C. Compare to C2C or C2W technology, only one cycle bonding process (heating-up with load force) is applied in this step, which markedly reduces the risk of MEMS and IC failure.

The preliminary results demonstrated that the proposed method is promising for MEMS ubiquitous applications in wireless sensor network and other consumer products.
High-Throughput UV Nanoimprint Process Using Flexible Replica Mold for High-Brightness Light-Emitting Diodes

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Keywords: UV nanoimprinting, resin mold, light emitting diodes

This paper demonstrated a high-throughput fabrication process of replica mold and nanostructures for high-intensity light-emitting diodes (LED). The fabrication process includes roll-to-roll (RtR) UV imprinting for replica mold fabrication and perpendicular UV imprinting on wafers. Figure 1 shows flow diagram of the developed equipment for high-throughput UV imprinting (ST-50LED, Toshiba Machine Co., Ltd.). UV imprinting on wafer is carried out continuously by using the flexible replica mold fabricated by RtR imprinting. A stocked wafer and rolled replica mold are transferred to a vacuum chamber and UV-imprinted under a reduced pressure. The used pattern in the mold is rolled and the new pattern area is supplied to the chamber. The throughput is higher than 30 wafers/hour. Figure 2 shows photograph and scanning ion microscope (SIM) image of the imprinted samples. The pattern was formed on the whole area in the silicon wafer. The imprinted pillar pattern is $184 \pm 3 \text{ nm}$ in diameter, $219 \pm 3 \text{ nm}$ in height, and $283 \pm 2 \text{ nm}$ in pitch. The measurement results suggest that the replica mold was uniform enough to use for subsequent UV imprinting, and highly uniform UV imprinting was achieved by means of the developed equipment. Thickness of the residual layer within a wafer was shown in Figure 3. The averaged thickness was $31 \pm 2 \text{ nm}$. This result indicates that the thickness is highly uniform and repeatable.

Replica molds fabricated by RtR imprinting is expected to be cost-effective because the RtR process is suitable for mass-production. If the replica mold is disposable, some problems for multiple uses such as contaminant accumulation, deformation of patterns, and reduction of releasability are expected to be negligible. This fabrication process is expected to be applied to fabricate nanostructures for actual high-intensity LEDs.

Fig. 1. Flow diagram of developed high-throughput UV imprinting equipment.

![Flow diagram of developed high-throughput UV imprinting equipment.](image)

Fig. 2. (a) Photograph and (b) SIM image of a UV imprinted sample.

![Photograph and SIM image of a UV imprinted sample.](image)

Fig. 3. (a) Thickness of residual layer within a wafer and (b) cross-sectional SIM image of the pattern at $x = 15$. 

![Thickness of residual layer within a wafer and cross-sectional SIM image of the pattern.](image)
High-sensitivity Leak-testing Method with High-Resolution Integration Technique

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Keywords: leak-testing method, leak-rate, helium gas, sensor package, mass spectrometer

1. Introduction

A high-resolution leak-testing method named HR (High-Resolution) Integration Technique has been developed for MEMS (Micro Electro Mechanical Systems) sensors such as a vibrating angular-rate sensor housed in a vacuum package. Procedures of the method to obtain high leak-rate resolution were as follows. A package filled with helium gas was kept in a small accumulation chamber to accumulate helium gas leaking from the package (Figs. 1, 2). After the accumulation, the accumulated helium gas was introduced into a mass spectrometer in a short period of time, and the flux of the helium gas was measured by the mass spectrometer as a transient phenomenon. The leak-rate of the package was calculated from the detected transient waveform of the mass spectrometer and the accumulation time of the helium gas in the accumulation chamber (Fig. 3, Eq. 1). Because the density of the helium gas in the vacuum chamber increased and the accumulated helium gas was measured in a very short period of time with the mass spectrometer, the peak strength of the transient waveform became high and the signal to noise ratio was much improved.

The detectable leak-rate resolution of the technique reached $1 \times 10^{-15}$ (Pa·m$^3$/s). This resolution is $10^3$ times superior to that of the conventional helium vacuum integration method (Table 1). The accuracy of the measuring system was verified with a standard helium gas leak source. The results were well matched between theoretical calculation based on the leak-rate of the source and the experimental results within only 2% error.

$$Q = \frac{S'}{t_s \cdot \left(\frac{P}{P_0}\right)}$$

Whereas;
$Q$: Leak-rate (Pa·m$^3$/s)
$t_s$: Accumulation time
$S'$: Total helium gas quantity
$P$: Helium gas pressure sealed in package
$P_0$: Standard pressure

![Image 1](Configuration of HR Integration Technique)

![Image 2](Photograph of main parts)

![Image 3](Derivation total quantity of leakage helium gas from the transient waveform)

<table>
<thead>
<tr>
<th>Methods</th>
<th>Evacuation time $t_0$ (min)</th>
<th>Resolution (Pa·m$^3$/s)</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>JIS helium vacuum integration method</td>
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<td>$1 \times 10^{-12}$</td>
<td>1</td>
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<tr>
<td>HR Integration Technique</td>
<td>10</td>
<td>$1 \times 10^{-15}$</td>
<td>$1 \times 10^3$</td>
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</tbody>
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Table 1. Comparison of detectable leak-rate between HR Integration Technique and helium vacuum integration method
MEMS Wafer-level Packaging Technology Using LTCC Wafer

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Keywords : LTCC wafer, MEMS, Wafer-level packaging, Anodic bonding, Hermetic packaging, Electrical connection

Wafer-level hermetic packaging with electrical feedthroughs is one of key common technologies for MEMS. Among many methods which have been developed to date, a borosilicate glass wafer with electrical feedthroughs offers the opportunity of reliable MEMS hermetic packaging by anodic bonding. However, its fabrication has the following difficulties. First, there is no good way to fabricate high-quality via-holes in a sufficiently-thick borosilicate glass wafer at high yield. Second, via-filling with metal is not easy and its hermetic reliability is sometimes problematic. Third, the via configuration is basically straight so that MEMS design flexibility is limited.

To solve the above problems, we have developed a novel LTCC wafer anodically bondable with Si. This LTCC is well matched with Si in the coefficient of thermal expansion (CTE), and contains sodium ions movable at elevated temperature of 360-400°C. Figure 1 shows the cross section of the LTCC wafer. It is made of a stack of punched green sheets, and paste-based Au vias and lines are formed through and between the stacked layer, respectively. Thus, multi-layer electrical feedthroughs can be embedded in the LTCC wafer. We confirmed the reliability of hermetic packaging using a Si diaphragm method and no significant change of diaphragm deformation was observed even after thermal shock test (−40 °C × 30 min / +125 °C × 30 min), as shown in Fig. 2.

To practically apply the LTCC substrate to a variety of MEMS, the electrical connection between them should be established by a simple and reliable method. We have developed a new electrical connection method shown in Fig. 3. The Au/Pt/Cr electrode on the MEMS substrate and the Au via in the LTCC substrate are connected by porous Au bumps, which are formed by wet etching the LTCC substrate to make a cavity. During the wet etching, the filler in the Au via is also etched away, leaving pores in the exposed Au via (Fig. 4), i.e. Au bump. In the bonding process, the porous Au bumps are mechanically pressed by projected electrodes on the MEMS substrate, and then anodic bonding is performed seamlessly. Using this method, 100% yield of both electrical connection and hermetic sealing was demonstrated. The thermal shock test (−40 °C × 30 min / +125 °C × 30 min) was performed up to 3000 cycles to these samples, and confirmed no significant changes in the resistance of the Daisy chain and the diaphragm deformation.

Fig. 1. Cross-sectional SEM image of the anodically-bondable LTCC substrate

Fig. 2. Diaphragm deformation during thermal shock test (−40 °C × 30 min / +125 °C × 30 min)

Fig. 3. Process of anodic bonding with electrical connection using the LTCC substrate for the wafer-level hermetic packaging of MEMS

Fig. 4. Surface and cross-sectional SEM images of a Au via (Au bump) in the etched cavity