Dynamic Power Consumption Optimization for Inductive-Coupling based Wireless 3D NoCs

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Abstract: Inductive-coupling is yet another 3D integration technique that can be used to stack more than three known-good-dies in a SiP without wire connections. Its power consumed for communication by inductive coupling link is one of big problems. A dynamic on/off link control for topology-agnostic 3D NoC (Network on Chip) architecture using inductive-coupling is proposed. The proposed low-power techniques stop the transistors by cutting off the bias voltage in the transmitter of the wireless vertical links only when their utilization is higher than the threshold. Meanwhile, the whole wireless vertical link will be shut down when the utilization is lower than the threshold in order to reduce the power consumption of wireless 3D NoCs. Full-system many-core simulations using power parameters derived from a real chip implementation show that the proposed low-power techniques reduce the power consumption by 43.8–55.0%, while the average performance overhead is 1.4% in wireless topology-agnostic 3D NoC.

Keywords: inductive-coupling, wireless, 3D NoCs, irregular topology, on/off link

1. Introduction

Due to the increase in the design costs of custom System-on-Chips (SoCs) in recent process technologies, System-in-Packages (SiPs) or 3D ICs that can be used to select and stack necessary known-good-dies in response to given application requirements have become one of promising design choices. Various interconnection techniques have been developed to connect multiple chips in 3D IC packages: wire-bonding, micro-bump [1], [2], wireless interconnects (e.g., capacitive- and inductive-coupling) [3], [4], [5], [6] between stacked dies, and through-silicon via (TSV) [3], [7] between stacked wafers. Many recent studies on 3D IC architectures have focused on micro-bumps and TSVs that offer the largest interconnect density. However, we consider inductive-coupling that can connect more than three known-good-dies without wire connections to be yet another 3D integration technique, because it provides a large degree of flexibility in building target 3D ICs, such as enabling chips in the package to be added, removed, and swapped after the chips have been fabricated, similar to what is done with building blocks.

A novel wireless 3D Chip Multi-Processor (CMP) architecture, in which the numbers of processor chips and cache chips in the same package can be customized for a given application set has been studied [8]. In such systems, if the application set requires more cache capacity or bandwidth, we can add more cache chips to satisfy such demands. If the target application set has more thread-level parallelism, we can add more processor chips to improve performance. Traditional wired Network-on-Chips (NoCs) are used as intra-chip networks in the proposed wireless 3D CMPs, while inter-chip communication is based on wireless inductive-coupling. Since a wireless 3D CMP is a collection of various chips provided by different vendors (e.g., memory, processor, and GPU vendors), we cannot expect to know any pre-determined network topology for intra-chip communications; this makes it difficult to establish routing paths that are free from deadlocks in such ad-hoc 3D CMPs. First, ring-based NoCs were proposed [9] and are available in a real heterogeneous multicore system with wireless interconnect [10]. Since the simplest ring networks cannot support enough performance, more generalized irregular networks were proposed [8].

Although the inductive-coupling itself is energy-efficient (e.g., 0.14pJ per bit [5]), inductors continuously consume a certain amount of power, regardless of packet transfers. That is, inductors waste significant power especially when the utilization of vertical links (i.e., inductors) is low, which is a typical use case of 3D ICs that the most communications are within a chip while the communications between chips are infrequent. Such power can be reduced by shutting down the link through controlling bias voltage of transistors used in the transmitter and receiver. Of course, since the shut down links cannot be used, the control must be done so as not to cause the performance degradation nor traffic congestion. Although simple techniques for dynamic power control were proposed in our previous paper [11], they are dedicated only for ring based network. Here, we propose generalized link on-off techniques for wireless NoCs with irregular network topologies. The rest of this paper is organized as follows. Section 2 presents the proposed wireless 3D NoC architecture in Ref. [8]. Section 3 proposes a dynamic power consumption optimization method for vertical links (inter-chip). Section 4 de-


scribes the results we obtained from evaluations and Section 5 concludes the paper.

2. Wireless 3D NoC

Figure 1 outlines the general wireless 3D NoC architecture, where the baseline 2D CMP is divided into four chips, each of which has four tiles, i.e., four processor tiles or four cache tiles. Wired links are used for the horizontal network that connects the four tiles on each chip, while wireless inductive-coupling links are used for the inter-chip network that vertically connects four chips. Each tile has a single processor (light blue box) or four shared L2 cache banks (pink boxes), in addition to a single on-chip router (red box).

2.1 Inductive Coupling Link

Inductive-coupling [3], [5], [6], [12] is a die-level wireless interconnection that uses square coils as data transmitters. Inductive-coupling has potential as an interconnection technology for custom building-block SiPs, since it can stack a number of examined dies wirelessly. That is, addition, removal, and swapping of hardware components (e.g., processor and memory chips) become possible after the chips have been fabricated and stacked in a package with a low cost. Inductive-coupling techniques have improved to the extent that a contact-less interface without an ESD protection device has been shown to be able to handle bit rate of more than 1 GHz with a low energy dissipation (0.14pJ per bit) and a low bit-error rate (BER $< 10^{-12}$) [5]. Although wireless inductive coupling has been utilized several systems: contactless memory card [13], a 3D dynamic reconfigurable processor [12] and a permanent storage system [14], we focus on a wireless link used in a 3D NoC.

An inductor is implemented as a square coil with metal in common CMOS layout. The data modulated by a driver are transferred between two coils placed at exactly the same position of two stacked dies, and they are received at the other chip by the receiver.

A uni-directional vertical link is consisting of a data transmitter (Tx), a data receiver (Rx), a clock transmitter and a clock receiver. The digital signal is serially transferred through Data Inductors synchronized with the local clock sent through Clk Inductors. For high throughput data transmission, high frequency clock is locally generated; for example, in Cube-0 [9], 4 GHz clock is utilized and by using both edges, 8 Gbps data transmission is possible. 32-bit digital data are serialized in MUX/DEMUX, and transferred in each 200 MHz system clock with 2-clock latency.

Since the inductor itself can be used both for transmitter and receiver, a half-duplex bi-directional link is formed by providing control mechanism to switch the direction.

The footprint of an inductor ranges from $30 \times 30 \mu m$ [5], [6] to $150 \times 150 \mu m$ [3], depending on the process technology and communication distance (i.e., chip thickness). Although it is much larger than the size for TSV, we can implement digital circuits inside the inductor.

2.2 NoCs with Wireless Interconnect Links

2.2.1 Ring-based Networks

The simplest way to build a NoC with wireless interconnect is using a uni-directional/bi-directional ring structure. Figure 2 shows the case of uni-directional ring structure. Adding, removing and replacing chips are easily done in the ring network. For further flexibility, the Bubble Flow control [9] is introduced to allow any intra-chip networks. From the viewpoint of practical implementation, chips are stacked with a certain length of gap so that the Tx channel is located exactly on the same place of the Rx channel of the next chip. The gap is also used for another important reason: keeping the space of bonding wires for supply voltage, ground and a system clock for synchronization.

Now, a heterogeneous multi-core system using the ring based NoC is available [10]. Although the ring networks are suitable as the first step NoC in wireless inductive coupling, the scale is limited because of its long latency stretched with the number of stacked chips. A generalized NoC architecture which allows any intra-chip network is proposed [8].

2.2.2 Generalized NoCs for Wireless Interconnect

In the general NoC, chips are vertically connected with the following rules: 1) all chips must have inductors at pre-determined locations. 2) The inductors are connected to input and output ports of on-chip routers to form vertical links, and 3) all the hardware components are topologically reachable to at least an on-chip router that has a vertical link. Any pre-determined network topology is not expected for each chip if these rules are satisfied. The total network in the system is treated as a spanning tree, and Up*/Down* routing; a topology-agnostic routing algorithm without virtual channels is applied.

It avoids deadlocks in irregular topologies without virtual channels, based on the assignment of direction (up or down) to network channels [15]. Figure 3 has two examples of spanning trees, each of which has a different spanning tree root (node 0 or 7). A legal path must traverse zero or more channels upward followed by zero or more channels downward to guarantee free-

Fig. 1 Wireless 3D NoC architectures.

Fig. 2 The uni-directional wireless ring network.
In order to select an appropriate root node, [8] proposes a root node selection algorithm. Needless to say, the location of a spanning tree root significantly affects the hop count and utilization of links. For example, the routing path from nodes 2 to 5 in Fig. 3 (a) employs a non-minimal path, because the minimal path is prohibited by the spanning tree whose root is located at node 0; thus, four hops are required to send a packet. However, the minimal path in Fig. 3 (b) is allowed by the spanning tree whose root is located at node 7; thus, only two hops are required. Here, we focus on the on/off vertical link method on this architecture as a standard NoC for 3D wireless interconnect.

2.3 Related Work

Link-on/off power control is popularly used for power saving of interconnection networks. Soteriou and Peh [16] explored the design space of on/off interconnection network based on a dynamic power management technique where network links can be turn on/off in response to bursts and drops in traffic with a distributes fashion. Kim et al. [17] proposed dynamic link shutdown (DLS) for cluster interconnection. It shuts off the power of down links when their utilization is below a certain threshold level, and a subset of highly used links can keep connectivity in the network. An adaptive routing strategy that intelligently uses a subset of links for communication was proposed, thereby facilitating DLS for minimizing energy consumption. In Ref. [18], more finer approach to divide and control the power domain is applied.

The above link-shutdown/wake-up control techniques for common NoCs are basically different from the link-shutdown/wake-up control for wireless inductive coupling. As shown in later, a power of the inductive coupling link is controlled by the bias voltage of the transistor in the driver and receiver. The overhead of power control is quite small and the latency is not so large.

On the other hand, in traditional power-gated NoC systems, the dedicated power control network is provided, since the NoC is used in the same chip. In wireless 3D NoCs, each chip is connected only with inductive coupling links and it is difficult to provide a dedicated network for the power control. Thus, once a receiver is in the sleep mode, it cannot check the status of the corresponding transceiver until it is woken up by the signal from another link in the same chip.

Our previous work [11] is the first one to tackle the system level power control of NoCs with wireless inductive coupling links. However, it only treats ring-based networks with poor scalability. Here, in this paper, we propose a link-on/off control for generalized NoCs with wireless inductive coupling.

3. Dynamic Power Consumption Optimization

Power consumption optimization is essential for inductive-coupling based wireless 3D CMPs. A novel optimization scheme is proposed in this section.

3.1 Power Consumption of Vertical Link and Problems

First, the power consumption of the target system (the vertical link described in Section 2.1) is analyzed. SPICE simulation is used for evaluation of the test chip Cube-0, since it is difficult to analyze the power consumption of inductive coupling link in a real chip. The inductive coupling link designed for a test chip Cube-0 [19] is used as a target vertical link. The circuit diagram of the inductive coupling link is shown in Fig. 4. By utilizing a 65 nm BSIM model in SPICE simulation, data rate and power dissipation for inter-chip communications (i.e., inductive coupling links) of four stacked chips were calculated. Cube-0 was implemented with e-shuttle 65 nm CMOS process, and mounted on a test print circuit board that was also developed to measure this real chip. The power consumption by the chip is calculated from the Ampere-meter and Voltmeter attached to the circuit board. By comparison, the total power of the simulation was almost the same value from a real chip. The power consumption of vertical link, on-chip router and communication controller are shown in Table 1. Here, “Active” mode shows the power when the data are transferred through the link, while no actual data are transferred in the “Idle” mode.

Compared with traditional works [20], [21], [22] using power gating on NoCs, we can clearly find that the power consumption of vertical link of wireless interconnection is large. This is due to the big gap between operating frequencies for routers and vertical links (200 MHz and 4 GHz respectively). Moreover, vertical links continuously consume a certain amount of power, regardless of packet transfers. There is big waste to energy when the utilization of vertical links is low, which is a typical use case of 3D ICs that the most communications are within a chip while the communication between chips are not frequent. For example, Table 2 shows ratio of idle time to application time in vertical links used in a full-system 3D CMP simulator which will be introduced in Section 4. For the vertical links, 86.7% of the application execution time is idle in average.

In “Sleep” mode, the transceiver is disabled by cutting the bias voltage supply. As shown in Fig. 4, a simple on/off switch is connected to current source (bias voltage is mostly used as voltage controlled current source) at both ends of DxData (i.e., transmit-
Fig. 4 Circuit of inductive coupling link.

<table>
<thead>
<tr>
<th>Table 1</th>
<th>Power consumption of on chip network components [uW].</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Vertical link</td>
</tr>
<tr>
<td>Data Transmitter</td>
<td>4,600</td>
</tr>
<tr>
<td>Data Receiver</td>
<td>3,500</td>
</tr>
<tr>
<td>Router</td>
<td>74.5</td>
</tr>
<tr>
<td>Communication Controller</td>
<td>700</td>
</tr>
</tbody>
</table>

Table 2 | Idle time ratio in vertical links [%].
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Benchmark programs</td>
<td>SP</td>
<td>MG</td>
<td>CG</td>
<td>BT</td>
<td>LU</td>
</tr>
<tr>
<td>Idle time ratio</td>
<td>98.1</td>
<td>83.9</td>
<td>95.6</td>
<td>76.7</td>
<td>86.5</td>
</tr>
</tbody>
</table>

3.2 On/off Algorithm for Vertical Links

In this paper, we assume that full-duplex vertical links are employed as communication model. Although spanning tree is a uni-directional kind of technique, here we assume that deadlock-free routings that use multi-spanning trees exist in our optimization. The deadlock-free routing uses spanning trees only for computing paths. Once path is computed, communication is done in full-duplex manner.

Since it just stops the transceiver or receiver for the inductive coupling link, the state transition between sleep mode and active mode does not require energy overhead except the power consumption in the controller. It is like the clock gating used in digital circuits, and not so related to power gating which requires energy overhead both for shutting down and activation. Moreover, the latency overhead of state transition between sleep mode and active mode is one clock cycle, same as the case between idle mode and active mode.

Two sleep modes are proposed here. Table 1 shows that the large part of power is consumed by the transmitter. So, if the transmitter for data (DTx) is shut down, a large part of power consumption can be saved. This mode is called partial sleep method (PSM). It only shuts down the data transmitter (DTx). Since other parts are running, the vertical link can be woken-up when the sender activates DTx in one clock cycle and sends the packets.

Another mode is full sleep method (FSM). In this mode, the whole vertical link including DTx, DRx, CTx, CRx, and CLclk transceiver will be shut down. Although the total analog part of wireless inductive link is shut down, the communication cannot be done until transceivers in both chips are woken-up.

We set a reasonable threshold utilization value first, then compare the link utilization within a sample window (time slot) with the threshold when flit transmission completes. If the utilization is higher than the threshold, the state of the target vertical link is set from active to PSM. Otherwise, if there are paths to wake up the whole vertical, we set the state to FSM. If not, PSM is used again to only shut down the DTx. The decision to turn on a vertical link is basically the converse of the sleep mechanism and can be done as on-demand because of the property of fast on/off link transition. Such on/off control flows are summarized in Fig. 5.

The sleep decision is based on the utilization of target vertical link and whether there are enough reachable paths to send wake up signals. Theoretically, every link can be used to wake up sleeping vertical links. For example, wake up signal can be sent through brother vertical link (routers are connected by a couple of links which are called brother links), neighboring vertical links, or remote vertical links.

As shown in Fig. 6, several paths (green arrows and yellow arrows) are available to wake up the whole sleeping vertical link (yellow box with capital x is Tx, dark green box with capital x is Rx). We can see there is only one path in Fig. 7. Meanwhile, there are more than one wake up paths in Fig. 6. However, we have to think about the balance between power saving and performance overhead instead of selecting an arbitrary path. The impact will be shown in Section 4.

In addition, a simple rule which can avoid the deadlock is introduced:

Rule 1: if there are one or more paths to send wake up signals, the whole vertical link can be shut down. Otherwise, we have to shut down the DTx only.

Obviously, our proposed on/off vertical links methods satisfy this rule. We prove as follows.

Proof:

(1) In ring approach, the only two neighbor vertical links between two layers would use each other to wake up DRx, CTx, and CLclk. Then, we cannot shut down these two vertical links simultaneously. One of them would check the other one’s state before shutting down the whole vertical link. If the other one’s state is FSM, then shut down DTx only (PSM). That is, the vertical link in PSM state makes sure that there is one path to send wake up signals.

(2) In irregular approach, we set at least one ever-on vertical link.
between two layers. This guarantees the connectivity of the inter-chip network. In other words, the ever-on vertical link avoids the network deadlock.

As shown in Fig. 8, for example, the red vertical link is set to ever-on link. The wake up signals will be transferred through the red vertical link if nearer vertical link cannot be found. The vertical link which has the highest utilization will be selected as ever-on link by the system after several clock cycles sampling. The ever-on link will be always in power-on state or PSM state no matter how the environment changes. Thus, at least one path is provided to transfer wake up signals.

Note that, data packets comply with Up/Down routing while wake up packets (i.e., signals) do not only comply with Up/Down routing. Since Up/Down routing forces packets not to transfer through some paths that may cause deadlocks, the system performance will be worse, if the wake up packets simply transfer by rule of Up/Down routing. Therefore, we consider two cases. (1) For neighbor vertical links, X-Z-X or Y-Z-Y routing is used. Figure 9 shows an example of path selection for waking up sleeping vertical link. Red lines and blue lines represent two spanning trees. If wake up packets transfer from node 14 to node 6, yellow path is prohibited by Up/Down routing, but allowed by X-Z-X routing. Thus, wake up packets have higher possibility to be transferred to destinations. (2) For remote vertical links, wake up packets are transferred according to Up/Down routing, and driven to transfer through ever-on vertical link. However, when nearer power-on or PSM state vertical link can be found before arriving...
ever-on vertical link, that power-on or PSM state vertical link will be selected to transfer wake up packets. Since the scale of target 3D NoC is small, we set only one ever-on vertical link between each two layers.

4. Practical Considerations and Experimental Results

Here, our main target is a generalized wireless network proposed in Ref. [8]. It is referred as “irregular approach” since it can cope with any network topologies. For comparison, we also show results of a single ring-based topology [11] as “ring approach.”

First, the target CMP architecture that has 16 and 64 tiles and its evaluation environments are described. Second, the power consumption by irregular approach and ring approach is evaluated. Finally, the proposed on/off vertical link methods will be applied to both approaches. The impact of the proposed on/off vertical link in irregular approach is evaluated in terms of the performance overhead and saving of power consumption. It is also compared with ring approach for reference. Note that, because of the limitation of layer numbers in ring approach, we only compare the case of 16 tiles (i.e., 8 layers in ring approach while 4 layers in irregular approach).

4.1 Target NoC Architecture and Evaluation Environments

Here, we assumed shared-memory NoCs, in which each chip has one processor, each processor has one private L1 data and instruction caches, while the unified L2 cache banks are shared by all the processors, as shown in Fig. 1. These processors (CPUs), L2 cache banks, and memory controllers (MCs) are interconnected via on-chip routers.

Table 3 shows the configurations for 16-tile and 64-tile wireless 3D NoCs. Topology \((x, y, z)\) denotes a wireless 3D NoC that consists of \(z\) chips where each chip consists of \(x \times y\) tiles. Figure 10 illustrates the irregular and ring topologies (we evaluate ring topology with 16-tile configuration) to be evaluated in this paper. The number of chips \(z\) is fixed at four in the irregular approach, while their sizes correspond to \((2,2)\) and \((4,4)\) for 16-tile and 64-tile NoCs.

We used a full-system CMP simulator that combines GEMS [23] and Wind River Simics [24] to simulate the wireless 3D CMPs. We modified a detailed network model inside GEMS, called Garnet [25]. The power parameters based on SPICE simulation are fed to the simulator. The results (network power consumption and application program execution time) of each evaluation can be automatically output after full-system simulation. The power consumption model will be shown in Section 4.2.2. That is, we can compare the results of network power consumption before and after power optimization for ring and irregular approaches, respectively. A directory-based MOESI coherence protocol that defines three message classes was used. Table 4 lists the processor and network parameters. We used parallel programs from the OpenMP implementation of NAS Parallel Benchmarks (NPB) [26]. Sun Solaris 9 operating system (OS) was running on the CMPs. These benchmark programs were compiled with Sun Studio 12 and were executed on Solaris 9 OS. The number of threads was set to four or eight, depending on the number of processors (e.g., four threads for 8-tile CMP).

4.2 Baseline Comparison between Irregular and Ring Approach

This section compares the irregular and ring approaches in terms of the application performance and power consumption.

Table 4 Simulation parameters (processor, memory, and network).

<table>
<thead>
<tr>
<th>Processor</th>
<th>UltraSPARC-III</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1 I/D cache size</td>
<td>64 KB (line:64B)</td>
</tr>
<tr>
<td>L1 cache latency</td>
<td>1 cycle</td>
</tr>
<tr>
<td>L2 cache bank size</td>
<td>256 KB (assoc:4)</td>
</tr>
<tr>
<td>L2 cache latency</td>
<td>6 cycle</td>
</tr>
<tr>
<td>Memory size</td>
<td>4 GB</td>
</tr>
<tr>
<td>Memory latency</td>
<td>160 (± 2) cycle</td>
</tr>
<tr>
<td>Router pipeline</td>
<td>[RC/VSA][ST][LT]</td>
</tr>
<tr>
<td>Buffer size</td>
<td>5-flit per VC (default)</td>
</tr>
<tr>
<td>Flit size</td>
<td>128 bit</td>
</tr>
<tr>
<td>Protocol</td>
<td>MOESI directory</td>
</tr>
<tr>
<td># of message classes</td>
<td>3</td>
</tr>
<tr>
<td>Control / data packet size</td>
<td>1 flit / 5 flit</td>
</tr>
</tbody>
</table>

Table 3 Irregular topologies to be tested (parameters).

<table>
<thead>
<tr>
<th>Topology</th>
<th>#routers</th>
<th>#CPUs</th>
<th>#L2$ banks</th>
<th>#Memories</th>
</tr>
</thead>
<tbody>
<tr>
<td>16-tile(ring)</td>
<td>(2,1,8)</td>
<td>16</td>
<td>4</td>
<td>32</td>
</tr>
<tr>
<td>64-tile( irr)</td>
<td>(2,2,4)</td>
<td>16</td>
<td>4</td>
<td>32</td>
</tr>
<tr>
<td>64-tile( irr)</td>
<td>(4,4,4)</td>
<td>64</td>
<td>8</td>
<td>128</td>
</tr>
</tbody>
</table>

Fig. 10 Irregular and ring topologies used in the evaluation part. In the ring topology, every chip has a horizontal link while only the top and bottom chip actually use it [9]. In the irregular topologies, horizontal links are randomly removed with 50% probability while vertical links are not removed.
One thousand irregular topologies were randomly generated for each CMP configuration to evaluate the irregular approach so that each horizontal link appeared with 50% probability while each vertical one appeared with 100%. Out of 1,000 trials for each network size, a network that had the closest hop count value to the average was selected for full-system CMP simulations. In addition, the irregular approach uses three VCs, so we call it Irr3 in this paper.

One or more spanning tree roots are selected with the proposed technique of optimizing spanning trees for each message class of applications using the cost function [8] to minimize the average hop count. Two configurations are used to compare with ring approach.

- **Irr3(max):** The worst spanning tree root that maximizes the average hop count is selected for each message class of each application.
- **Irr3(min):** The best spanning tree root that minimizes the average hop count is selected for each message class of each application.

In addition, Ref. [9] proposes to use Bubble flow control [27], [28] for the vertical ring so as not to use any VCs. It uses a single 15-flit FIFO buffer for each physical channel in order to store three packets in each buffer. Thus, its buffer capacity is equivalent to three VCs each of which has a 5-flit FIFO buffer. In summary, the following configuration of ring approach is compared with Irr3(max) and Irr3(min).

- **Ring:** Ring approach with Bubble flow control (15-flit FIFO for each physical channel)

### 4.2.1 Application Performance

Figure 11 shows the application execution time of NPB applications with the irregular and ring approaches on the 16-tile and 64-tile configurations. The execution time (Y-axis) is normalized so that the execution time in ring approach indicates 100% in Fig. 11. As expected, the irregular approach is better than the ring one that suffers due to poor scalability. The irregular configuration outperforms the ring one by up to 12.8% in terms of the application performance.

Up to here, we showed that the irregular approach outperforms the ring one in terms of the performance per cost.

### 4.2.2 Power Consumption

The most important contribution of this paper is improving the energy efficiency of the wireless 3D NoC by means of introducing two sleep modes. So we quantitatively compare ring and irregular approaches before and after using our proposed on/off vertical link methods. The following power model is used to calculate the power consumption of networks for these two approaches.

\[
P_{\text{NoC}} = P_{\text{router}} N_{\text{router}} + P_{\text{link}} N_{\text{link}} + P_{\text{clink}} N_{\text{clink}}
\]

where \(N_{\text{router}}\), \(N_{\text{link}}\) and \(N_{\text{clink}}\) represent the number of routers, horizontal links, and vertical links traversals on average. \(P_{\text{router}}\), \(P_{\text{link}}\) and \(P_{\text{clink}}\) correspond to the power consumption of a router, a horizontal link, and a vertical link. The \(P_{\text{router}}\) and \(P_{\text{clink}}\) are set according to Table 1, Section 3. For the \(P_{\text{link}}\), horizontal links take up 65% power consumption of the whole 2D NoC [29] while routers take up 35%. Therefore, the \(P_{\text{clink}}\) is set to 150 uW.

The power consumption comparison among the Ring, Irr3(max) and Irr3(min) is shown in Fig. 12. The power consumption (Y-axis) is also normalized so that the power consumption of Ring approach indicates 100%. As shown in Fig. 12, the Ring network with 16-tile configuration consumes the largest power, and it exceeds Irr3(max) by 12.9–15.3% and Irr3(min) by 14.1–16.0%, respectively. In the case 16-tile configuration, 28 full-duplex vertical links are employed in Ring network while 24 full-duplex vertical links are used in both Irregular networks. Thus, 14.3% more vertical links are employed in Ring network than in both irregular networks. Needless to say, more power is consumed by ring network. Meanwhile, the power consumption of the Iir3(max) is slightly larger than that of Iir3(min) but much smaller than that of Ring network due to the increased hop count.

### 4.3 Power Saving

In this section, we quantitatively compare the proposed approach with the conventional method (i.e., vertical link is going to be idle state when no flit comes). The conventional method is employed in Cube-0 [9] implementation. This method is applied to ring approach and irregular approach in 16-tile configuration.

For the flexibility of our proposed method, big power saving can be obtained. As shown in Fig. 13 (a), 23.4–28.7% power saving in ring approach while 43.8–50.0% in Irr3(max) and 46.7–50.9% in Irr3(min) are achieved. On average, 25.4%, 46.2% and 48.5% power consumption can be saved in Ring, Irr3(max) and Irr3(min), respectively.

As mentioned in Section 3, enough available paths are needed for sending wake up signals. Obviously, only one vertical link can
be shut down between two layers in ring approach. In irregular approach, by contrast, much more vertical links can be shut down because only one vertical link around the sleeping vertical link is needed to be awake. Since this vertical link is used to wake up the sleeping neighbor vertical link, other three vertical links around the sleeping vertical link can be shut down. Therefore, we can see in Fig. 13(a), our proposed on/off link methods applied to irregular approach can obtain 20.8% more power saving than applied to ring approach on average. As seen in Fig. 13(b), irregular approach with 64-tile can save more power consumption, but not so much.

In general, our proposed method applied to Irr3(min) can save more power than Irr3(max). According to our paper [8], 25.2% and 31.4% more hops are generated by Irr3(max) than Irr3(min) based on 16-tile and 64-tile configurations, respectively. Undoubtedly, the utilization of some vertical links will increase because of more hop counts. In terms of our proposed method, PSM is used when vertical link utilization is higher than a certain threshold while FSM is used in the case of lower utilization. And FSM can save much more power than PSM. From the above, Irr3(min) has more opportunity than Irr3(max) to use FSM, but not PSM. As shown in Fig. 13(a) and Fig. 13(b), Irr3(min) can save 2.3% more power consumption than Irr3(max) on average.

4.4 Performance Overhead

Commonly, power saving techniques cause a certain performance degradation. Figure 14(a) and (b) shows how much performance is degraded by the proposed methods.

As shown in Fig. 14(a) application performance degrades by 0.1–2.4% in ring approach while 0.8–2.2% in Irr3(max) and 0.4–3.3% in Irr3(min). On average, the application execution time can be 0.6%, 1.3% and 1.5% longer than the time before using our proposed method in the Ring, Irr3(max) and Irr3(min), respectively. The results demonstrate that performance overhead of the proposed methods is quite small. Note that, the performance overheads are different among application programs. For example, in “CG” and “BT” which require a lot of data exchanges, the performance of Irr3(max) will become much worse than that of Irr3(min). By contrast, in other application programs, there are a small amount of data exchanges.

Again, it’s clear that we could find many paths to wake up a sleeping vertical link according to the proposed method. There is only one path to wake up sleep vertical link in ring approach (i.e., neighbor vertical link). However, remote vertical links can be used to wake up the sleeping vertical link. The following equation shows the latency to wake up a sleeping vertical link.

\[ T_{\text{latency}} = T_{\text{router}} N_{\text{router}} + T_{\text{link}} N_{\text{link}} + T_{\text{link}}. \]  

(2)

where, \( N_{\text{router}} \), \( N_{\text{link}} \), and \( N_{\text{link}} \) represent the number of routers, horizontal links, and vertical links traversals on average. \( T_{\text{router}} \), \( T_{\text{link}} \), and \( T_{\text{link}} \) correspond to the latency by transmitting wake up signal via a router, a horizontal link, and a vertical link. Apparently, the latency to wake up a sleeping vertical link in ring approach is smaller than in irregular approach. Because the \( N_{\text{link}} \)
is sometimes more than one in irregular case while equals to one in ring case. On average, in the case ir3,min with 16-tile configuration, 0.9% more performance overhead is caused than in the ring case.

5. Conclusions

One of the most important problems of NoCs using 3D wireless inductive coupling link is its power consumed for communication by inductive coupling link. A dynamic on/off link control for topology-agnostic 3D NoC architecture using inductive-coupling is proposed. The proposed low-power techniques stop the transistors by cutting off the bias voltage in the transmitter of the wireless vertical links only when their utilization are higher than the threshold. Meanwhile, the whole wireless vertical link will be shut down when the utilization is lower than the threshold in order to reduce the power consumption of wireless 3D NoCs.

Full-system many-core simulations using power parameters derived from a real chip implementation show that the proposed low-power techniques reduce the power consumption by 43.8–55.0%, while the average performance overhead is 1.4% in wireless topology-agnostic 3D NoC.

Now, power control mechanism works only dynamically. Considering the application property, the static on/off mechanism is advantageous since the target network allows any type of topologies. Shutting down of some links stastically for the target applications will save much power without performance overhead. Combination of such a static control and dynamic control proposed here is our future work.

References

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