2-D Motion Vector Detection Sensor

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[Abstract] In this paper, we propose a high speed 2-D motion vector detection sensor with the edge detection, double array digital memory, and block matching of the binary edge information are integrated on a focal plane. The processing unit is composed of analog processors with pixels parallel structure and the digital processors with column paralle structure. The first prototype chip is designed under the process of 1.5 μm CMOS technology with a fill factor of 17 % and with the die size of 7mm × 7mm.

1 Introduction

The motion vector detection usually requires high computational complexity in conventional image processing system. Here in this paper, we propose a computational sensor integrated on a focal plane sensor with the ability of high speed 2-D motion vector detection.

2 Motion Vector Detection Scheme

A higher frame rate, for instance, 1000 frames per second, makes discrepancies very small between two successive frames. Motion vector detection scheme can be simpler for higher frame rate images. Thus, we attempt to realize very fast motion vector detection integrated on the focal plane. The motion vector detection is based on 1) binarization by edge detection and 2) block matching of the binary edge information. Although the algorithms are simple, they are effective for implementation on the tiny focal sensor plane.

3 Focal Plane Processing Architecture

The processing architecture is in a way of column parallel, and it makes use of a sort of mixed analog and digital processing, as illustrated in Figure 1.

4 Design of motion detection sensor

4.1 Edge Detection Algorithm

Here in our design, by using of the differences between neighboring horizontal and vertical pixels[1], a simple edge detection algorithm can be used for the approximation of the detailed local changes of high speed 2-D moving pictures. As shown in Figure 2, it consists of the image sensing circuit and the 2-value level edge detection circuit.

\[
\begin{align*}
\Delta_1 & = f(i, j) - f(i + 1, j) \\
\Delta_2 & = f(i, j) - f(i, j + 1)
\end{align*}
\]

\[E = |\Delta_1| + |\Delta_2|\]

4.2 Digital Memory Array

The output of the edge detection signal is put into the digital edge memories. Here we devised the digital memory array with a size of 31x31 for storing the edge information from the current frame and from the previous frame. With this double array structure, the edge information is stored into the memory array conveniently.

图2: Edge Detection Algorithm

图3: Double array digital memory

图1: Architecture of 2-D motion vector detection

1. transducing
2. the horizontal and vertical edge detection
3. 2 memory arrays for storing current and previous frame information
4. a matching operation between current and previous frame memories
5. digital and analog output of the best matched vector.
4.3 Block matching by Absolute Difference and Accumulation

The block matching is conducted between $2 \times 2$ pixels ($W_{\text{current}}$) in current frame and corresponding pixels ($W_{\text{pre}}$) in previous frame. Block matching is illustrated in Figure 4. Within a search area of $\pm 1$ in horizontal and vertical direction, the controlling signals $c_{\text{left}}, c_{\text{center}}, c_{\text{right}}$ moves the window $W_{\text{pre}}$ left and right, and the read out signal of the edge information moves the window $W_{\text{pre}}$ up and down but operates repeatedly 3 times for reading 3 lines' edge information. After these 9 times operations, 9 matching values $\{y_1, y_2, y_3, \ldots, y_9\}$ are produced, which are sent to the accumulator while they are being produced. Since every $y_i$

4.4 4-bits D/A converter

Only 1 D/A converter is needed for converting the column parallel digital codes into serial analog signals. Instead of an Opamp, in Figure 7, here we use a simple PMOS amplifier at the output of the DAC. By a proper design of the W/L parameters of the transistors, a relatively satisfied result can be got. As shown in Figure 8, although the output signal has a little difference from its designed value and the dynamic range becomes a little smaller, the changes are tolerable.

5 Summary

In this paper, the algorithm principle, function architecture such as the double array digital memory, and the whole design procedure of the 2D motion vector detection sensor are presented. The processing unit is composed of analog processors with pixels parallel structure and the digital processors with column parallel structure. The first prototype chip is designed under the process of 1.5 µm CMOS technology with a fill factor of 17 % and with the die size of 7mm $\times$ 7mm.

参考文献
