a-Si Gate Driver Designs for Low Power AMLCD Operation

(低消費電力アクティブマトリクス液晶ディスプレイ駆動のためのa-Siを用いたゲートドライバの設計)

Keitaro Yamashita[†], Toshiya Inada[†], Steven Deane^{††}, Paul Collins^{††}, Satoshi Kawata[†],
Yasuyuki Onda[†], Masahiro Yoshiga[†], Jason Hector^{††} and Masahide Inoue[†]

Abstract We have developed two 1.8" QVGA (222dpi) transfective a-Si AMLCDs with integrated gate drivers. One is optimized for a very low power normal operating mode. The other can switch to an arbitrary partial scan mode. Gate driver integration results in narrow, symmetric margins, reduced cost, and fewer interconnections. Also, we minimized the number of connections to the display while retaining some to achieve very significant power reduction.

Keywords : Amorphous silicon TFT, Gate Driver, Low Power Consumption, Partial Scanning, Shift Register, Long Lifetime

1. Introduction

In mobile AMLCDs one of the key specifications is the power consumption of the display. This can be split into a number of parts. The backlight is usually the highest consumer of power, but the power required to address an image onto the display is also significant. If the display is transfective, the power consumption to address the display when the backlight is switched off is clearly important, particularly in mobile applications. This requirement makes a low power gate driver a necessity at the backlight off state, as well as the source driver with low power mode.

Gate driver designs in a-Si technology have been studied^{1) 2)} and these can be placed on the active plate, reducing the number of row side connections from 320 to approximately 10-20 for a portrait QVGA display case³⁾. In this paper we present two enhanced a-Si gate driver designs that can, again, be made in a standard a-Si process and reduce the power required to address the display.

The first driver makes use of increased numbers of clock phases and 3-level voltage drive to reduce power, at the expense of the number of drive signals required. We targeted a total gate driver power of less than 1mW for a QVGA display in normal addressing mode and this is

reasonably competitive in mobile applications to date. The second design is an implementation that allows the display to be addressed in a partial display mode. The number of rows addressed can be arbitrarily chosen and also the starting row position of the addressed portion can be arbitrarily addressed. This combination of features makes the driver very suitable for telecom applications.

2. Low power gate driver

The first step in optimizing the gate driver power consumption is to understand the lifetime factors affecting the circuit. By making the circuit elements larger, we can enhance the lifetime, at the expense of increased power consumption. Thus, we need to be able to accurately understand the circuit driver operation over its lifetime to design a circuit with enough lifetime, without wasting power on an unnecessarily long lifetime. The lifetime-power trade off can be chosen depending on application requirements.

The circuit architecture of the gate driver also has a significant effect on power consumption. In **Fig. 1** the block diagram of a very low power a-Si gate driver is shown.

The external driver feeds 18 signals to operate the gate driver. These consist of 12 clocks, 4 other control pulses and 2 power lines. In the gate driver the capacitive load includes parasitic loads on each of the clock lines, and this consumes power at each transient on the clock line. Increasing the number of clock lines reduces the power

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[†] TPO Displays Japan K.K.

(4-3-1 Takatsukadai, Nishi-ku, Kobe 651-2271, Japan)

^{††} Philips Research Laboratories

(Cross Oak Lane Redhill Surrey RH1 5HA, UK)

consumption in the gate driver, because the number of transients per line is reduced by the distribution of pulses.

Fig. 2 shows an example of clock lines and branches connected to shift register cells. Assuming here to use 3-phase clocks in QVGA display, the total number of capacitor connected to one clock line is expressed by approximately:

$$C_L \approx 320/3 \cdot C_{SR} \quad (1)$$

where, CSR is cell input capacitor value.

When we use 6-phase clocks, total capacitance value per clock line will be approximately:

$$C_L \approx 320/6 \cdot C_{SR} \quad (2)$$

The power consumption is proportional to the total capacitor value. Thus, by doubling the number of clock phases, we can approximately halve the gate driver power consumption.

Clearly, a balance must be chosen between the num-

Fig.1 Gate driver block diagram showing total drive signals required.

Fig.2 Gate driver block diagram by 3-phase drive clocks and 6-phase drive clocks case.

ber of interconnect lines and the power consumption, and this can be chosen according to customer wishes.

Fig. 3 shows the driving timing chart for the gate driver for low power. The cyclical clock pulses are distributed to 6 phases in this case. Every clock line feeds a pulse every 6 rows, so that the power consumption in gate driver can be reduced.

Fig. 4 shows the gate driver power consumption dependency on the number of phases of driving clock lines. The power consumption is reduced by the increased number of clock phases. We achieved a low power consumption of 0.69mW at 60Hz for QVGA mobile display.

Further power saving can be made if the clock transitions are modified by creating a third selected level at ground making three level waveforms. **Fig. 5** shows a typical circuit that may be used to generate the three level voltage waveforms, and the detail of the waveforms as they are switched via the ground (GND) level in every transient from low (VGL) to high (VGH) and vice versa.

The driving power of the conventional two level driving is given by:

$$W_C = fCE(E - U) + fCU(U - E) \quad (3)$$

where, C is line capacitor value, E is gate high voltage level, U is gate low voltage level and f is frequency. In case of 3-level voltage driving, when the clock line is connected to GND, then the existing charge on clock line is discharged to GND without consuming power. After the voltage level has reached the GND level, again the clock line is charged up to high level or low level. The power in the 3-level voltage driving is given by:

Fig.3 Drive signal timing required for the integrated gate driver.

Fig.4 Graph showing the effect on power consumption of the number of clock phases supplied to the gate driver assuming for 1.8" QVGA, +17.5/-12.5V, 60Hz frame rate.

Fig.5 Drive signal expanded waveform detail illustrating a typical "3-level" drive generation circuit and output waveform.

$$W_C' = fC(E^2 + U^2) \quad (4)$$

The total power consumption of the gate driver is proportional to the number of charge and discharge events. By using 3-level voltage driving operation, the power in a clock line is reduced by the factor of 1/2 if the absolute

Table 1 Main module parameters.

Parameter	Value	Unit
LCD Type	a-Si colour TFT/ Normally White Transflective	
Active area	27.4 x 36.5	mm
Resolution	240 (xRGB) x 320	pixels
Pixel	38 (xRGB) x 114	μm

voltage swings, high and low, are the same. We realized approximately 46% of the theoretical power reduction by using 3-level voltage drive with voltage levels of +17.5V and -12.5V for VGH and VGL respectively. This measured value is reasonably consistent with calculations.

Table 1 shows the main parameters of a display made with this very low power gate driver designed according to the above principles, and **Fig. 6** shows an image from the display. It can be seen that there is no compromise in display performance caused by this power optimization.

Another route to achieve very low powers is to have a partial display mode, where only a small portion of the display is addressed. This architecture is mainly used in stand-by mode.

Fig. 7 is the illustration of partial display mode to reduce system power consumption. In this mode, it is useful if the partial area, number of rows and location can be chosen freely, so we have designed a second novel gate driver design to achieve this.

This gate driver allows us to arbitrarily select the driven gate lines, and even two separate partial display regions could be chosen. The power consumption in the source driver can also be significantly reduced by not

Fig.6 An image of a display with the low power integrated a-Si gate driver operating with 16M colours.

Fig.7 Illustration of partial display mode.

addressing the undriven the sections.

Fig. 8 describes the block diagram of the partial scanning gate driver. This gate driver consists of shift driver cells, output buffer cells and partial enable switches. The gate driver is designed to achieve a long lifetime by considering the transistor stress caused by the continuous addressing.

Fig. 9 shows measured row pulses for the gate driver operating in normal scan mode and partial scan mode.

As this novel gate driver is designed to have a flexible partial scanning mode, either the normal scan mode or the details of the partial scan can be programmed by the controller. In this measurement a partial display mode where four gate lines were selected starting at row 4 was chosen as an example. Since our partial scanning gate driver showed the same output pulses as the conventional partial scanning gate driver, it is possible to maintain the image quality in partial scan mode with previously

Fig.8 Partial display capable gate driver block diagram showing signals required for operation.

Fig.9 Two graphs showing measured row pulses for the gate driver operating in normal scan mode (top) and partial scan mode (bottom) .

introduced methods⁴⁾⁻⁶⁾.

Fig. 10 shows the measured effect on power consumption of the gate driver of the number of lines driven in partial mode and the start position of the driven rows. There is a proportional relationship between the gate driver power consumption and the number of lines driven in partial scan mode.

Fig.10 Graph showing the measured effect on power consumption of the gate driver of the number of lines driven in partial mode and the start position of the driven rows.

Generally the power consumption of the gate driver is much smaller than that of source driver, however partial scan mode also produces a reduction in source driver power consumption. Especially in stand-by mode, the partial scan mode can significantly reduce the system power consumption. In a QVGA with 64rows driven case, it is expected that the total power consumption is reduced to a few milliwatts and this is approximately 20% of the power consumption in normal mode. This contributes to maintaining battery life.

3. Conclusion

We have made a 1.8" QVGA (222dpi) transfective a-Si AMLCD with an integrated gate driver and a partial scanning gate driver compatible with normal scanning. Gate driver integration results in narrow, symmetric margins on the display, reducing cost, fewer interconnections and also lower module power consumption in stand-by mode by partial scanning. We have demonstrated a flexible partial scan gate driver, which has been an issue for previous attempts to make an a-Si gate driver.

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Keitaro Yamashita He graduated from Doshisha University, Kyoto, Japan in 1997, and received B.S in electronics. Since 2002, he has been engaged in development of advanced AMLCD in TPO Displays Japan (former Philips Mobile Display Systems). His recent work is in the field of system on panel using LTPS and aSi technology for telecom and automotive application.

Toshiya Inada He received his M.S. degree in chemical engineering from the Himeji Institute of Technology in 1987. He joined Hosiden in 1987 as AMLCD design engineer. After transferred to Philips Mobile Display Systems Kobe K.K. In 2000, he has still worked as designer of various AMLCDs in TPO Displays Japan.

Steven Deane He graduated from Cambridge University, UK, in 1992 with a PhD in thin film electronics. Since then he has been involved in research for large area electronics, in particular a-Si AMLCDs and AMOLEDs for both mobile and TV applications.

Paul Collins He graduated from the University of Southampton, England in 2002, and received a 1st class Masters Degree (MEng) in Electronic Engineering. Sponsored through his degree by Philips Research, he began working in the field of LTPS AMLCDs, and more recently amorphous Si Gate on glass technology.

Satoshi Kawata He received his B.S in chemistry from Kyoto Institute of Technology, Japan in 1993. He joined TPO Displays Japan (former Philips Mobile Display Systems Kobe K.K) in 2002. He is working as an electrical engineer for TFT displays.

Yasuyuki Onda He graduated from Fukuoka University, Japan in 1989, and received B.T. in electrical engineer. Since 2004, he has been engaged in development of AMLCD in TPO Displays Japan (former Philips Mobile Display Systems). His work is in the field of AMLCD driving scheme technology for telecom and automotive application.

Masahiro Yoshiga He received his B.S. And M.S. degrees from Kyoto Institute of Technology, Japan, in 1991 and 1993, respectively. He joined Hosiden in 1993 and transferred to Philips Mobile Display Systems Kobe K.K. In 2000. He is engaged in front of screen performance in TPO Displays Japan.

Jason Hector He completed research for a PhD in the field of spectroscopy of doped GaLaS glasses which was awarded by the University of Southampton in 1998. Since joining Philips Research Laboratories in 1999 he has been working in large area electronics for AMLCD, AMPLD and image sensors.

Masahide Inoue Senior Architect/Global Advanced Technology/TPO Displays Japan. Received Bachelor degree in Applied Chemistry from Himeji Institute of Technology/Japan in 1987. Joined TPO Displays Japan (former Hosiden Corp.) in Apr 1987. Leading Advanced Technology Development as Senior AMLCD Architect.