An On Chip Negative High-Voltage Generator

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Abstract

In this paper, we propose new charge pump circuits utilizing CMOS with capacitors to generate negative high-voltage. Circuit operation and characteristic are discussed and compared. With cross-coupled CMOS topology, the new circuit can generate negative output voltage without suffering from threshold voltage drop of the MOS transistor. Therefore, the circuit can offer better voltage pumping gains and suitable for low voltage operation and good property in voltage regulation.

I. Introduction

Charge pumps are the circuits that can pump charge upward to produce voltage higher than the power supply voltage. The circuit can be made small and integratable because regenerative component such as inductor becomes not necessary. This may be a reason why on-chip high-voltage generators become more popular and increasingly incorporated on many LSI and VLSI chips. Charge pump circuits are generally required in the single-supply nonvolatile memories, such as EEPROM and Flash memory, require the high-voltage generator for programming the floating-gate switches. Most high-voltage generators are based on Dickson charge pump [1] that can be implemented in various ways. Strait forward using of MOS, no matter N or P chain, one may suffer from device threshold voltage drop. On one hand, the amount of threshold voltage is dominant when the supply voltage is around one or two volts. On the other hand the more stage cascaded the more $V_{TH}$ drops. This is the limitation and the reason why the pumping gain cannot be made very high.

Cross-coupled CMOS inverter can be used as switches in charge pumping circuit. Devices operate in non-saturation mode that $V_{DS}$ drop are less than $V_{TH}$ drop. Such a circuit is investigated in this paper. Rather than focusing only on the details of a new negative high voltage generator, in addition and comparison, we also have investigated other 2 types of conventional negative voltage generator. Several parameters of the circuits are taken out. These are, for instance, number of stages, range of supply voltage, clock frequency, steady state times and output loading characteristic.

II. Circuit Configuration

A conventional single chain negative voltage generator with NMOS charge pumping circuit is shown in Fig. 1. This is, in fact, a slight modified version of the original Dickson’s pump. A double chain topology is depicted in Fig. 2. Although two-phase clocking is still employed, clock arrangement is alternated. Because of its parallelism the second circuit seem to have higher current drive (lower output resistance). In fact the improved conventional circuits in Fig. 2 can generate output voltage slightly higher than the conventional. Due to the ripple voltage of improved circuits are half of conventional circuits. Note that the substrate of NMOS devices are tied to the most negative voltage. This can ensure the less substrate bias influence. MOS Devices are working in the saturation mode and as diodes. The output voltage of the circuit shown in Fig. 1 can be given by (1)

$$V_{OUT} = -(n+1)V_{DD} + (n+1)V_{TH} \quad (1)$$

where $V_{TH}$ is the threshold voltage of NMOS modified by the body effect due to the source voltage. Obviously, the output voltage suffers from MOS threshold voltage which is also get multiplied by the number of stages when the output voltage $V_{OUT}$ is taken of.

The above drawback can be compensated by the proposed CMOS circuit shown in Fig. 3. The schematic diagram of such a circuit is similar to the CMOS positive charge pump proposed in [4]. It consists of two parallel paths having symmetrical CMOS structure and driven by two non-overlapping clock signal. $C_{K}$ are the kick capacitors, $C_{L}$ and $R_{L}$ are load capacitor and load resistor respectively. This circuit does not suffer the body effect because the source and the substrate terminals of each MOS are connected. It should be noted that MOS transistors operate in non-saturation region. The voltage at the end of 1st stage
can be calculated as \(-V_{\phi} + 2V_{DS}(L/fC_K)\). Therefore, the output voltage \(V_{OUT}\) of the n-stage circuit is approximately given by

\[
V_{OUT} = -nV_{\phi} + 2nV_{DS} \frac{nI_c}{fC_K}
\]  

(2)

where \(V_{\phi}\) is the voltage amplitude of clock signal and \(V_{DS}\) is drain-to-source voltage of MOS transistors. Since the \(V_{DS}\) is very small, the negative output voltage proportionally increases with the number of stage \(n\).

III. Simulations

To verify the operation of the proposed circuit and to compare the achievement to the conventional circuit, we did simulation with HSPICE. Device models are drawn from a double-well high voltage process [4] and given here again in Table 1. Despite the loading current and design rule violation, devices feature size can be reduce to their area optimal design, i.e. \(W/L=2/1\) and \(W/L=1/1\). Throughout many experiments we assume the output load \(C_i\) and \(R_o\) to be 100pF and 10Mohms respectively. Kick capacitors are assumed to be 5pF, clock voltage are varied from 0.5v to 2v at 2MHz clock frequency.

IV. Result

The simulation results are shown in Fig. 4 to Fig. 10. Clearly seen, with the same number of 20 stages, the proposed circuit can generate negative output voltage at about -17V from a 1V clock, while the conventional can reach as high as -7V. Fig. 5 shows the output voltage of the conventional and proposed circuit according to clock voltage variation. The maximum difference of the output voltage produced by conventional and our circuits seem to appear when the supply voltage is between 1 to 2 volts. When the supply (or clock voltage) made higher this gap reduces slightly. One also can notice that the proposed circuits offer a notably linear change at the slope (gain) of about 13.5V/V at 15 stages. We also examined the output steady time of those circuits since such an obtain can indicate when the output is suitable to be used. To get the 100% steady, it seems to be too long and not essentially necessary in the real application. We thus, measure the steady time at 90% of maximum value. Shown in Fig. 6, the output steady time is compared to the number of stages. For lower number of stages the proposed circuit can generate the output voltage in a very fast manner compared to the conventional circuit. While for the higher number of stages the proposed circuit yields the similar characteristic to the conventional circuit. The value of about 350us should sufficient for most applications. In Fig.7, when the kick capacitors are made change from 1 to 8pF, in all case less output change can be observed from the conventional circuit. Theoretically we can make as high as value of capacitors, but in practical VLSI circuit the value of semiconductor capacitor cannot be very high. The similar trend can be obtained when we investigated the change in clock frequency. The circuit shows less change in their output voltage when clock frequency is above 2 MHz. However, higher clock frequency may lead to more circuit power loss.

Fig. 9 and 10 demonstrate the loading characteristic of the circuit, started from similar voltage value, while observing the changes we have drawn different amount of load current. The proposed circuits show lower output resistance. This graph also confirms the better performance we can get from an improved conventional circuit (Conv.B) compared to its original one (Conv.A). We can increase the amount of circuit supply current (\(I_{OUT}\)) practically by increasing the value of kick capacitor. These can reach a few nano Farads for the range of mAs supply current. However, increasing the kick capacitor will result in the steady times to be longer. Such an application may also require off the chip capacitors [5]. Too less capacitor leads to the increasing of ripple voltage.

V. Conclusion

With the support theory and the obtained results, the proposed CMOS charge pump circuit for negative on-chip high voltage generator can show most desirable performances compared to the conventional versions. The most distinctive rule is that the proposed circuits work in non-saturation mode. Generally \(V_{DS}\) is lower than \(V_{TH}\) that also can be influenced by substrate bias. In our approach, \(V_{BS}\) are kept at zero, i.e., \(V_{BS}=0\). Similar result can be obtained when \(V_{BS}\) is made reverse bias, i.e. substrate is tied to \(V_{DD}\).

References


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Fig. 1 n-stage conventional negative voltage pumping circuit (Conv. A).

Fig. 2 n-stage improved conventional negative voltage pumping circuit (Conv. B).

Fig. 3 Proposed n-stage negative voltages pumping circuit.

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Fig. 4 Number of stage vs. Output Voltage

Fig. 5 Supply Voltage vs. Output Voltage

Fig. 6 Steady State Time vs. Number of stages n
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Table 1: Device parameters.

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<th>Parameter</th>
<th>PMOS</th>
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<tr>
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<td>V</td>
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<td>$1.0 \times 10^{16}$</td>
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<td>V</td>
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Fig. 7 Output Voltage vs. Kick Capacitor

Fig. 8 Output Voltage vs. Clock Frequency

Fig. 9 Output Voltage vs. Load Current

Fig. 10 Output Voltage vs. Load Current