A Hybrid CMOS/CCD ISAS (Image Signal Accumulation Sensor)  
- Technical Feasibility -

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Abstract A new ultra-high-speed image sensor “Hybrid CMOS/CCD ISAS” is presented. ISAS stands for "Image Signal Accumulation Sensor". A folded CCD is installed in each pixel, which serves as an in-situ memory for parallel recording at all pixels. The CCD is looped so that image signals captured at plural of capturing operations are automatically accumulated on the memory CCD. A CMOS readout circuitry is also installed in the pixel for fast and flexible signal readout. By directly reading out signals through the CMOS readout circuit without recording them in the in-pixel CCD memory, the sensor works as a conventional parallel and partial readout high-speed imager as well. A set of Z-shaped electrodes is proposed to fold the CCD and fabricate it with a standard CMOS process. Therefore, the sensor can be fabricated solely with a CIS process. Technical feasibility of the sensor is confirmed through simulations.

Keyword Ultra-high-speed, High sensitivity, Signal Accumulation, CMOS, ISIS, ISAS

1. Introduction
Etoh et al.\textsuperscript{1)} developed an ultra-high-speed video camera which can capture images up to 1 million frames per second (Mfps) in 2001. The video camera mounted an image sensor with a special structure known as ISIS, the In-situ Storage Image Sensor.

Since then, the design of ISISes has been continuously improved to achieve a much higher working frame rate\textsuperscript{2)} and sensitivity\textsuperscript{3)-4)}. In 2010, we successfully developed the ISIS-V16, which can operate at 16 Mfps\textsuperscript{5)}.

In ultra-high-speed imaging, there are cases in which the signal level is comparable with or less than the noise level. If the target events are reproducible, the simplest method to obtain reliable results is to repeat the experiments and average the accumulated data.

We propose the ISAS, the Image Signal Accumulation Sensor\textsuperscript{3)}, which is a special ISIS capable of accumulating image signals on-chip. A key feature of this design is in the use of a multi-folded storage CCD in each pixel with a direct connection of the first and the last elements, which enables the accumulation. We presented practical configurations for a two-phase and four-phase transfer ISAS using a conventional CCD process\textsuperscript{3)}.

However, the following limitations hinder us from developing the CCD-ISAS:

(1) There is a high possibility of stringer formation at the edge of the intersection between the first and second poly-Si layers. The residual poly-Si leads to electrical shorts between a couple of electrodes. To avoid this problem, CCD element size has to be sufficiently large and thus the number of stored images and the spatial resolution reduce.

(2) The two-phase ISAS is relatively easy to implement by using only one poly-Si layer. However, full well capacity is much less than that of a four-phase transfer.

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{figure1.png}
\caption{Four-phase transfer ISAS: (a) Using a two-poly-Si CCD process; (b) Using a one-poly-Si CMOS process.}
\end{figure}

With the advancement of CMOS fabrication technology,
a CCD can be made with poly-Si electrodes very close to each other. If the gap is sufficiently narrow, the gate potentials of adjacent electrodes overlap. As a result, a signal charge packet can be transferred smoothly and effectively across the electrodes. We now can produce an image sensor with a CCD memory in each pixel and a CMOS readout circuitry by using a deep-sub-micron CMOS process. The image sensor functions both as an ISIS to achieve ultra-high-speed and a parallel/partial readout (PPR) image sensor to achieve fast and flexible readout. Furthermore, using this approach, we can take full advantage of the continuous scaling of CMOS processes to achieve a smaller pixel size and more storage elements.

In this paper, we propose an innovative design with a set of Z-shaped electrodes to fold the CCD memory. The design requires only one poly-Si layer, which is suitable for a conventional CMOS image sensor (CIS) process with minor modifications. Technical feasibility of the ISAS is confirmed through device simulations.

2. ISAS structure

2.1. General structure

The photoreceptive area of the ISAS consists of 480x360 pixels. Each pixel has the size of 30x30μm² and can store 126 frames. The design frame rate is 10 Mfps. To achieve very high sensitivity, we use three existing technologies: backside illumination technology (BSI), cooling and large pixel size.

The expected performance indices are estimated by simulations and shown in Table 1.

<table>
<thead>
<tr>
<th>Table 1 Design performance of the Hybrid ISAS</th>
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<td>Max frame rate</td>
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<td>Pixel count</td>
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<tr>
<td>Pixel size</td>
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<tr>
<td>CCD element size</td>
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<td>Number of stored images</td>
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<td>Full well capacity</td>
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<td>Grey level</td>
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<td>On-chip signal accumulation</td>
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A fundamental pixel consists of four main parts as follows:

1. A CCD storage. A plurality of CCD elements is installed in each pixel to store more than 120 signal frames.
2. A CCD signal control area on the bottom right of a pixel in Figure 2(a). Various gates in this area can be controlled separately to form different operation modes.
3. A separation ring to separate CCD and CMOS areas.
4. A CMOS source follower readout circuit on the top right of a pixel.

![Figure 2. Pixel architecture of the Hybrid ISAS](image)

2.2. Poly-Si structure

We propose a new design which effectively avoids the stringer formation problem. The design only requires one poly-Si layer. Details of the solution are as follows:

1. Multiple Z-shaped electrodes are used to form the four electrodes of a four-phase transfer CCD.
2. Contacts are placed on the channel stoppers to
avoid unwanted barrier heights, which might cause insufficient transfer.
(3) At each connection, two contacts are placed instead of one. This implementation will improve the fabrication yield of the chip.
(4) Simulation results show that sufficient fringing fields can be obtained even with a 0.27μm-gap. The actual gap used in our design is 0.18μm for a 0.11 μm CMOS process.
(5) Metal layer 1 comprise of multiple groups, each with four horizontal wires to supply power for multiple Z-shaped poly-Si electrodes.
(6) One CCD fold is shortened to give space for a p-well contact in each pixel.

2.3. Separation ring
In this design, there is a strong n-type separation at the boundary of the CCD memory and the CMOS readout within a pixel, thus, leads to a loss of pixel space and the lowered fill factor. However, this separation is necessary because p-wells of the CCD and CMOS are biased differently. P-wells in CMOS parts are grounded while those in CCD are biased at a negative voltage to achieve our optical requirement shown in Table 1.
an ISIS such as: ultra-high-speed image capturing, low noise, but it also has disadvantages such as: a limited number of frames and limited full well capacity.

In both ISAS and ISIS modes, after an image capturing operation stops, charge signal is transferred to the floating diffusion via the OG gates and converted to a voltage by a CMOS readout circuit installed in each pixel.

3.3. PPR mode

In this mode, the ISAS functions like a conventional high-speed PPR image sensor. A charge packet is sent to the floating diffusion directly via the shortcut gates (SC) without going to the in-pixel CCD memory.

In this mode, practically an unlimited number of frames can be captured at high speed with much larger full well capacity due to large pixel sizes. On the contrary, the maximum image capturing speed reduces to less than 10,000 fps and noise level is higher than those in ISAS/ISIS modes.

4. Simulation

Simulation studies are conducted to optimize the channel potential profile and full well capacity. To achieve efficient charge transfers, a voltage swing of 5.5V is necessary, which is only one third of that of the previous ISISes. A CMOS imager process typically offers a gate oxide thickness from 8nm to 20nm, which is 2.5 to 6 times smaller than that from a CCD process (about 50nm). Therefore, we can expect 30% to 70% reduction in total power consumption.

A CCD storage element has the size of 1.6x3.2μm². An electrode pitch is 0.8μm including a 0.18μm-space. The full well capacity is estimated to be about 5,500e-. It is suitable for most practical ultra-high-speed applications, since we cannot expect much incident light to the sensor at 1Mfps and above.

We also carefully design the fold part of the CCD to achieve sufficient transfer efficiency. Simulation results at a fold of area B in Figure 2 are shown in Figure 4. Using a standard 4-phase transfer with 50% duty cycle, a charge packet is transferred effectively along the fold in three operations. First, A2 and A3 electrodes are biased HIGH while A1 and A4 electrodes are kept LOW (Figure 4(a)). Second, A2 electrode is biased LOW while A4 electrode is biased HIGH (Figure 4(b)). Lastly, A3 electrode is biased LOW and A1 electrode is biased HIGH (Figure 4(c)).

5. Conclusion

We propose an Ultra-high-speed Hybrid CMOS/CCD ISAS. It is an ISIS with the function of on-chip

Figure 4. Channel potential at a fold of area B shown in Figure 2(b). Arrows indicate the proposed charge transfer along the fold: (a) A2 and A3 are HIGH; (b) A3 and A4 are HIGH; (c) A4 and A1 are HIGH.

summation of image signal sequences for a series of image capturing operations without reading out the captured image signals out of the sensor.

The ISAS can operate at 10 Mfps as an ISIS and at 5-10 kfps as a conventional parallel readout image sensor. The sensitivity is about several photons per pixel by application of BSI technology.

A new poly-Si electrode design is proposed, which consists of a set of organized Z-shaped electrodes to achieve the multi-folded CCD structure. The whole sensor can be fabricated solely with a CIS process with minor modification such as the addition of specified implants to improve the full well capacity of the sensor.

The simulation study has proven the possibility and the validity of the sensor.

References