A Novel Charge Recovery Logic Structure with Complementary Pass-transistor Network

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1 Introduction

In this paper, a new charge recovery logic structure [1] called Complementary Pass-transistor Boost Logic (CPBL) is proposed. CPBL is a low-power logic structure powered by 2-phase non-overlap alternating power clocks and requires no DC power supply. To demonstrate the energy efficiency of CPBL, 4-bit counter is designed to show the energy comparison between CPBL and the conventional static CMOS with 0.18µm CMOS process. The simulation results indicate that CPBL implementation reduces about 65% power dissipation compared with the static CMOS counterpart in a range from 50MHz to 500MHz.

2 Complementary Pass-transistor Boost Logic

Fig 1 shows a cascade of three CPBL buffers and output waveforms of buffer1 and buffer2. Each CPBL gate operates in two stages, Logic and Boost. When Logic evaluates, Boost does not drive the outputs and vice versa. Consider the operation of buffer2 whose inputs and outputs are shown in Fig 1(b). The voltage swing of power clock is from 0 to $V_{DD}$. During the Logic stage, power clock pc and pc_b are in low half cycle and high half cycle respectively. As such, Boost stage is in cut-off and the clocked transistors M5 and M6 turn on, evaluated logic values can be transferred to output nodes. With the inputs of buffer2 boosted by buffer1 to $V_{DD}$, the complementary pass-transistor network charges the out2 to approximately $V_{DD} - V_{th}$ and discharges the out2 to the GND and there is a little voltage difference between output nodes achieved by the end of the Logic stage.

As pc rises and pc_b falls, buffer1 and buffer2 transition into Logic stage and Boost stage respectively. Since the outputs of buffer1 become low and M5, M6 are turned off, Logic part is decoupled from output nodes. During the first half of Boost stage as pc goes up, since out2 is at $V_{DD} - V_{th}$ and out2 is GND, transistor M3 turns on first, causing out2 to follow the pc to $V_{DD}$, reaching approximately 1V. With the rising of out2, transistor M2 turns on subsequently, out2 is still connected to the GND. In this way, Logic value “1” and “0” are boosted to full rails to drive the Logic stage of buffer3. In the second half of Boost stage, because transistor M1 is in cut-off all along during this stage, charges at the out2 are recovered as power clock pc falls down.

3 4-bit counter simulation and comparison

To demonstrate the performance of CPBL, we present simulation results of CPBL 4-bit counter [2]. For comparison purposes, the simulation results of the conventional static CMOS counterpart are also shown with the same Rohm 0.18µm process technology.

4-bit counter consists of 4 T flip-flops and 2 AND gates. However, the CPBL signals have timing constraint that output signals have half cycle delay compared to input as shown in buffer cascade. Therefore, the charge-recovery flip-flops cannot be built by just using the conventional static CMOS structure. The characteristic equation for T flip-flop is $Q_{n+1} = Q_n \oplus T$, so CPBL T flip-flop can be built by a XOR gate and an AND gate which is used to achieve Reset function. Also, we clock these two gates with complementary power clocks pc and pc_b.

Fig 2 shows the energy comparison in a frequency range from 50MHz to 500MHz. CPBL counter reduces about 65% energy compared to the static CMOS implementation.

References
