Advanced Microwave Integrated Circuits with Ceramic Integration Technologies

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The highly integrated monolithic microwave power amplifier module for W-CDMA (wideband code division multiple access) cellular phones were designed and fabricated taking advantage improvements in microwave materials and new developments in processing methods of thin films for applications in decoupling capacitors and choke inductors. The obtained module is ultimately downsized into 3.0 mm by 3.5 mm with 0.5 mm in thickness. The volume is about 10 times smaller than that of the ceramic chip components assembled conventional power amplifier module.

Key-words: Thin film, Ceramics integration, Power amplifier, Microwave module

1. Introduction
The growth of commercial and consumer wireless markets have caused to realize smaller and lighter handset with passive chip components downsized to 0402 case-size (1.0 mm × 0.5 mm × 0.5 mm).[1]-[4] However, the need for a large number of passive chip components for impedance matching and filtering for high-frequency circuitry is still getting to increase.[5] While integration has reduced the number of the semiconductor chips, similar integration has not occurred for passive components, which occupy a major fraction of board area, and contribute significantly to component and assembly cost. Also, the majority of wireless equipment has used conventional printed circuit board technologies, with some extension in their capabilities to handle the frequencies required. However, it is becoming increasingly clear that such technologies do not address all the technical and commercial needs of the market. Printed circuit board technology has a number of limitations for packaging and interconnects in wireless applications. Specifically, the dimensional stability of polymer materials is poor, with CTE's (coefficient of temperature expansion) of 20 ppm/°C or greater, and poor stability in a humid atmosphere, which leads to moisture absorption, and changes in board dimension and electric properties. The dielectric loss associated with such materials results in high attenuation in microwave components, leading to poor component performance and diminished battery life. Such problems become more significant as frequency is high. What is needed is a technology offering low loss, mechanically and electrically stable components and circuits. Technology which integrate passive components into the LTCC (low temperature co-fired ceramics) substrate, providing a single interconnect and package entity with controlled impedance elements and fewer solder joints would give designers new tools to decrease size, lower cost and improve reliability.[5],[6] And further, final solution for cost reduction and downsizing of high-frequency circuitry is obviously one-chip solution using monolithic microwave integrated circuit (MMIC) technology.[7] However, at present MMIC has a number of limitations for designing high-frequency circuitry as one-chip solution from passive circuit formation technology points. The capacitors are usually deposited SiO2 or Si–N amorphous thin films with stable and well-established semiconductor planer technology which exhibit very low dielectric constant, as the result, it is unable to obtain large capacitance on restricted GaAs or Si die size. This means that by-pass capacitors and decoupling capacitors can not be designed onto the die, consequently, MMIC needs external ceramic chip capacitors for by-pass and decoupling of the circuits. In a same way, 2-dimensional spiral inductors fabricated onto the die cannot obtain larger inductance value, because the 2-dimensional spiral structure for large inductance needs unacceptable occupation area on the semiconductor die. In addition, the structure cannot make high-density magnetic flux, which can be realized by 3-dimensional spiral structure as shown in multilayer ceramic chip inductor for high-frequency use.[8],[9] Therefore MMIC needs external choke inductors as ceramic chip components form. Above mentioned external ceramic chip components include un-controllable parasitic elements, these tolerance decreases the production yield of wireless devices in mass production stage.

We approached that designing and fabrication of highly integrated monolithic microwave power amplifier module for W-CDMA (wideband code division multiple access) cellular phones, in which decoupling capacitors and choke inductors were already built as thin film form and transistors were buried into Si substrate using MEMS (micro electro-mechanical system) technology. We introduce this unique circuit designing procedure in this technical note.

2. Design of module
2.1 Structure of the module
Figure 1 shows the conceptual figure of the module. A cavities for burying a GaAs power transistor was formed onto high-resistance Si substrate (4 kΩ cm) with SiO2 surface insulating layer using deep chemical etching method which is usually adopted for bulk MEMS fabrication. Input, inter-stage (between pre-amplifier and power amplifier) and output impedance matching circuits were built up with
multi-layered structure on the substrate: first, high capacitance SrTiO₃ MIM (metal insulator metal) capacitors for by-pass and decoupling capacitors, low-capacitance SiO₂ MIM capacitors for adjustment of impedance and Ni-Cr thin film resistors were deposited onto the substrate with Al-Cu/Au transmission lines, then further deposition of ferromagnetic thin film and Al-Cu/Au conduction lines including spiral patterns for inductors was formed after the polystyrene inter-insulating layer formation. The ferromagnetic thin film located beneath the spiral conduction pattern can dense magnetic flux and increase inductance value of the spiral inductor. Each conduction patterns and passive elements were electrically connected with Al-Cu/Au conduct plugs and they formed 3-dimensional multilayer circuit. Finally the power amplifier module was completed by mounting 2-stage (consisting of pre-amplifier and power-amplifier) GaAs HBT (heterojunction bipolar transistor) exhibiting high power efficiency and high linearity with compact die size into the cavity and its electrical connection to the circuit with Au wire bonding.

2.2 Circuit design

The specification required to power amplifier modules for W-CDMA mobile handset is shown in Table 1. The specification was regulated for high-speed and wide-band wireless communication as the third generation cellular phone system, Therefore, it is indispensable for its power amplifier module to satisfy not only high power efficiency but also high linearity. As they are usually inconsistent, designing of impedance matching circuits is critical to achieve such tough specification. We designed input and inter-stage matching circuits to obtain the maximum output power, and more carefully designed output impedance matching circuit to achieve both high linearity and power efficiency. Generally for the output impedance matching, empirical and very sensitive tune is required to obtain optimized balance between linearity and efficiency. Linearity of power amplifier for digital modulation reflects to ACPR (adjacent channel power ratio). HPSK (hybrid phase shift keying) modulation is adopted for W-CDMA up-link and its peak to power-average ratio of signal is about 3.5 dB. It is necessary that the output back-off at operating point of the module is over 3.5 dB in order to realize well-depressed ACPR. However, high efficiency is the most high priority subject for the module. Therefore, it is indispensable for its power amplifier to satisfy not only high power efficiency but also high linearity. As they are usually inconsistent, designing of impedance matching circuits is critical to achieve such tough specification. We designed input and inter-stage matching circuits to obtain the maximum output power, and more carefully designed output impedance matching circuit to achieve both high linearity and power efficiency. Generally for the output impedance matching, empirical and very sensitive tune is required to obtain optimized balance between linearity and efficiency. Linearity of power amplifier for digital modulation reflects to ACPR (adjacent channel power ratio). HPSK (hybrid phase shift keying) modulation is adopted for W-CDMA up-link and its peak to power-average ratio of signal is about 3.5 dB. It is necessary that the output back-off at operating point of the module is over 3.5 dB in order to realize well-depressed ACPR. However, high efficiency is the most high priority subject for the module. Therefore, it is indispensable for its power amplifier to satisfy not only high power efficiency but also high linearity. As they are usually inconsistent, designing of impedance matching circuits is critical to achieve such tough specification. We designed input and inter-stage matching circuits to obtain the maximum output power, and more carefully designed output impedance matching circuit to achieve both high linearity and power efficiency.

As the results, this power-amplifier is operated in class-AB. Figure 2 shows the schematic circuit diagram of designed module.

2.3 SrTiO₃ thin film capacitors

The by-pass capacitors and de-coupling capacitors are used for control of the power supply variation and the circuit stabilization in all circuits. SrTiO₃ thin film MIM capacitors exhibiting dielectric constant of 280 are applied to the circuits, which are large enough for the by-pass and de-coupling capacitors of high-frequency modules. The RF impedance characteristics of the MIM capacitor with 100 µm² electrode size indicated in the Smith chart is shown in Fig. 3. The MIM capacitor works well as capacitor up to 3 GHz. As one example of the MIM capacitor, in order to reduce the input impedance of bias lines at 100 MHz, 470 pF SrTiO₃ MIM capacitors were applied to the circuits. Even though such larger capacitance was required, the occupation area was only 180 µm². Also we realized that maximum operation voltage of power amplifier was about 7 V by analyzing its load lines, therefore the thickness of SrTiO₃ was decided as 150 nm.

2.4 High-frequency choke inductors with magnetic thin film

In general, DC power is supplied to active devices through choke inductors. However, increase of inductance value of thin film spiral inductor inevitably increases the number of turns and results not only increase of occupation area on semiconductor dies, but also increase of series resistance which causes degradation of Q (quality) value of inductor. We have already developed nano-granular magnetic thin film which is applicable to high-frequency range. The inserting magnetic thin film beneath the spiral inductor succeeded to increase the inductance 20%
RF leakage to the bias lines and its resultant voltage drop were prevented by the inductors. 15 nH of inductors were applied as choke inductors in the circuits. The size of this inductor was 380 \( \mu \)m by 420 \( \mu \)m, \( Q_{\text{max}} \) is 5.2 at 330MHz and series resistance is 2.54 \( \Omega \).

2.5 Transmission lines and high Q spiral inductors

The total quality of MMIC circuits is strongly depending upon the quality of transmission lines. The less resistance value is preferable for high-frequency circuits. Also, less dielectric constant of inter-insulating layers is key to obtain high-frequency circuits. On our circuit designing case, wider and thick transmission lines were realized (44 \( \mu \)m of width and 4 \( \mu \)m in thickness), since low dielectric constant polyimide inter-insulating layer (\( \varepsilon_r \geq 2.9 \)) was adopted with enough thickness (21 \( \mu \)m). As the results, the designed circuits could obtain insertion loss of 0.1 dB/mm at 6 GHz. This multi-layered polyimide was also adopted for high-Q inductors for matching circuits with double-layer spiral structure as inter-insulating layers. The RF characteristic of double-layer spiral inductors is shown in Fig. 5 in comparison with that of single-layer spiral inductor. It clearly shows that the inductance per each unit length increases more than single-layer spiral inductor.

2.6 Layout and performance

The layout of the thin film module designed with aforementioned elements and circuits is shown in Fig. 6. The module could be fabricated with tremendous compact-size of 3.0 mm by 3.5 mm with 0.5 mm in thickness. It can be expected that further optimization of layout should realize more smaller die size to reduce the production cost. Moreover, thermal resistance of the module, defined as its temperature variation per total input power, should be suppressed to 1/5 compared with the alumina substrate based module, because the adopted covalent bonding Si single crystal substrate has excellent heat conductivity. Parameter extraction from each element in the circuit indicates the
fabricated module can exhibit the linear gain of 20.2 dB, the ACPR of $-41.8$ dBc, and the efficiency of 35.6% at Pout of 27 dBm. (Fig. 7).

3. Conclusion

We proposed and designed thin film passive integrated module by ceramic integration technologies. Also we fabricated thin film passive elements and established those process. It shows great potential for the future wireless devices through the innovation of the new materials for high-frequency applications, the optimization of process and the structures of devices, and appropriate circuits designing. The effective studies to fabricate and evaluate the module are going on. These results will be published somewhere else near future.

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