A High-Speed CMOS OP Amplifier with a Dynamic Switching Bias Circuit

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Abstract: This paper presents a high-speed CMOS operational amplifier (OP Amp) with a dynamic switching bias circuit, capable of processing video signals of over 2 MHz with decreased dissipated power. The OP Amp was designed to operate at a 10 MHz dynamic switching rate, and was shown in simulations to have a dissipated power of 66 % of conventional continuous operation. This OP Amp was applied to a switched capacitor (SC) non-inverting amplifier with a gain of 2, and its high-speed 10 MHz dynamic switching operation, capable of processing video signals, was demonstrated. By increasing the switching duty ratio to 70 %, its power dissipation decreased to 56 % of normal operation. Some inaccuracy in the SC amplifier performance resulted mainly from the limited open loop gain of the OP Amp. This circuit configuration should be extremely useful in realizing low-power wide-band signal processing ICs.

Key Words: video signal processing, switched capacitor circuit, CMOS, operational amplifier.

1. Introduction

Recent trends in the development of video signal processors for video electrical appliances have moved toward high speed and multi-functions. For example, high sampling rates, such as 10-20 MHz, are required for digital video signal processors to handle video signals, of which bandwidth is more than 2 MHz today. In spite of such exigent requirements, the throughputs of the processors have been brought into practical use owing to the development of parallel processing architectures and to the progress of short channel CMOS technologies. The integration of more multi-function systems into one chip monolithic IC is currently under the successive progress. Up to now, real time image processors with functions such as coding, vector quantization, motion compensation, filtering, edge detection, and so on, have been developed [1],[2]. However, the chip size of these processors is large and these have the disadvantage of operating at greatly large power dissipation of over 1 W. These also need A/D and D/A conversion circuits, which bring larger power dissipation when they are integrated with main processors.

On the contrary, the switched capacitor (SC) technology enables analogue signal processing without using any A/D and D/A conversion circuits, and has been mainly applied to the filters with low frequencies, such as a few hundred kHz [3]–[5]. Especially, the CMOS SC technology has promising use in video signal bandwidth circuits, because, by using the technology, one can easily integrate complicated systems into a single chip IC at low cost. In this paper, the author focuses on the SC technology because I believe it will enable low-power and high-speed operation. It was demonstrated that the SC techniques using CMOS operational amplifiers (OP Amps) are useful for implementing efficient measures with analog functions such as the filtering proposed in [6] and [7]. Although CMOS OP Amps are suitable for such filter ICs, the use of several OP Amps results in large power dissipation (causing unstable operation). Recently, a high speed CMOS OP Amp consisting of a fully differential operational transconductance amplifier (OTA) with two-pair’s folded-cascode OP Amps and a common-mode-feedback (CMFB) circuit has been developed [8]. This fully differential two-stage OTA was applied for high-gain and high-speed operations of SC applications, and demonstrated a low power dissipation of 10 mW at a high slew rate of 340 V/μs with a power supply voltage of 2 V. However, its circuit, which included several OP Amps, was too complicated for the signal processing IC, and so required a larger chip area and larger power consumption. Therefore, a simple circuit configuration, which enables smaller power dissipation and smaller chip area even when the number of the included OP Amps increases, is desirable for large-scale ICs of analog signal processing with multi-functions.

Until now, several approaches including the development of ICs working at low power supply voltages have been taken to decrease the power consumption of OP Amps. To decrease the power consumption of the OP Amp itself, a clocked current bias scheme for the folded cascode OP Amp has been proposed [9],[10]. In this circuit, each bias current for the slewing, settling, and holding phase is dynamically controlled by a multi bias current control method with clocked current sources. Even using this scheme, though, the maximum ratio of the total power savings is limited to about 30 %. Because the circuit also needs complicated four-phase bias-current control pulses and biasing circuits, it results in a large layout area and is not suitable for the high-speed operation.

Another approach to the low power dissipation, was an OP Amp with an adaptive common-mode-feedback (CMFB) circuit, which operates in a sub-threshold region, for improving its slew rate [11]. The adaptive bias circuit with a CMFB circuit is operated by dynamically enabling the bias current to adapt to the input signal. This OP Amp occupies a large layout area due to complicated control circuits. In this circuit, because all the MOSFETs operate in the sub-threshold region for lowering power consumption, the high-speed operation is difficult.

In this study, a novel CMOS OP Amp with a dynamic switch-
ing bias (DSB) circuit, of which configuration is simple, is proposed [12]. The circuit provides the low power dissipation while maintaining high speed switching operation suitable for processing video signals. This OP Amp can even operate at low supply voltages because of its non-cascode configuration. When the DSB circuit is also applied to the fully differential OTA or to the folded-cascode OP Amp, it can provide lower power consumption than the conventional ones by controlling the current source and/or the load using the DSB circuit. In addition, its circuit has not so complicated configuration, and offers the applicability to various kinds of OP Amp circuits with current sources for the control. The proposed circuit would contribute to lowering the power dissipation of OP Amp circuits.

2. Dynamic Switching Bias OP Amp

Figure 1 shows a CMOS OP Amp configuration with a DSB circuit. The OP Amp consists of a current-mirror differential amplifier M5–M9, an output amplifier with a coupling capacitor Cc, and a DSB circuit to dynamically turn the current source M5 and the output load M11 of the output amplifier, on and off. The coupling capacitor Cc is provided to prevent the OP Amp from oscillating or ringing. In the DSB circuit, an external control pulse $\phi_B$ with a voltage swing of (~5 V)–(+5 V) drives an inverting switching circuit consisting of the MOSFETs M1–M4. When $\phi_B$ becomes ~5 V, the buffer MOSFETs M1 and M2 set a bias voltage $V_B$ at an appropriate level by operating M3 and M4 in the saturation region. At this point in time, the OP Amp turns on and operates normally as an operational amplifier. In contrast, when $\phi_B$ becomes ~5 V, $V_B$ is set at nearly ~5 V, which turns off the current source M5 and the output load M11. The OP Amp does not dissipate any power during this off operation period. Thus, it is expected that the power dissipation of the OP Amp becomes significantly lower than in the usual continuous operation mode. The OP Amp operates successfully in a high speed switching mode because it does not use multi phase control pulses and current biasing circuits.

3. Simulation Results

The MOSFET and capacitor elements of the OP Amp were designed as shown in Table 1. Its characteristics were tested through SPICE simulations. The open gain and bandwidth of this OP Amp were 35.6 dB and 64 MHz. Figure 2 shows an output response waveform for 1 Vpp input pulse signal when used as a unity-gain buffer with a load capacitance $C_L$ of 10 pF. The slew rate of the OP Amp was 630 V/μs. The settling time (0.1 % and 10 pF) was 16 ns. This value is adequate to fully settle the switching operation at the 10 MHz switching rate.

The amplifier operated in a dynamic switching mode with a duty ratio of 50 %, a switching frequency $f_s$ of 10 MHz, power supply voltages $V_{DD} = V_{SS} = 5$ V and $C_L = 0.2$ pF when an input signal voltage $V_i = 0.01$ Vpp was applied as shown in Fig. 3. In this operation mode, the dissipated power was reduced to 66 % compared with the static operation mode (162 mW) at an input signal frequency below 2 MHz and $f_s = 10$ MHz (Fig. 4). The dissipated power in the output amplifier of the OP Amp constitutes nearly 50 % of the total dissipated power. Though this power in the on-state of the output amplifier is wastefully dissipated, this on-state period is extremely short (~50 ns) when operating at a high frequency such as at 10 MHz. Therefore, the on-state is needed for achieving sufficient charging or discharging of load capacitances within such a short period.

4. Switched Capacitor Amplifier

The author applied the OP Amp to an SC non-inverting amplifier which can be used for processing circuits such as filters. Figures 5 and 6 show its configuration and operation waveforms. The $\phi_1$ and $\phi_2$ switches consist of CMOS FETs with a channel width/ channel length W/L = 25/2.5 (μm/μm). Sampling pulses $\phi_1$ and $\phi_2$ complement each other. When the sampling pulse $\phi_2$ changes from a low to a high level, the amplified sampled input signal is output during the on-state of the OP Amp ($\phi_B$ is low). $\phi_B$ is set at low just before $\phi_2$ changes to high, such that the sampled input signal is amplified in a stable manner in the OP Amp. The $\phi_1$ fall and $\phi_2$ rise transitions were delayed for 10 ns after the $\phi_B$ fall transition (ΔT = 10 ns). Operation waveforms show that this amplifier with a gain ($= C_1/C_2$) of 2 can operate for a video signal bandwidth of over 2 MHz at $f_s = 10$ MHz (Fig. 7). The operation conditions were an input signal voltage $V_{in} = 1$ Vpp, an input signal frequency $f_s = 2$ MHz, $C_1 = 1.0$ pF, $C_2 = 0.5$ pF, and an output load $C_o = 0.2$
By increasing the dynamic switching duty ratio $T_B/T_s$ of the OP Amp to 70% at $f_s = 10$ MHz, its dissipated power $P_o$ decreased to 56% compared with the static operation (Fig. 8). That is, lower power dissipation is realized by using the DSB method. The accuracy of the output voltage is also important in practical applications. Figure 9 shows the output voltage inaccuracy versus the OP Amp switching duty ratio in the SC amplifier with a gain $(= C_1/C_2)$ of 2 at $f_s = 10$ MHz and $\Delta T = 10$ ns. The output voltage inaccuracy $\varepsilon$ represents the difference between the output voltage and a theoretical value ($gain \times input$ voltage). When the switching duty ratio $T_B/T_s$ is 0–70%, the inaccuracy $\varepsilon$ for the 1 Vpp input signal is within the range of 0.045 V–0.065 V (4.5%–6.5% of the theoretical value). The factors causing the accuracy to decrease are thought to be the static/dynamic characteristics of the OP Amp and sampling circuits.

To clarify the static inaccuracy of the OP Amp, the OP Amp was adapted as an inverting amplifier. Figure 10 shows the DC input voltage $V_i$ versus the output voltage inaccuracy $\varepsilon'$ in the inverting amplifier with a gain $R_2/R_1$ of 2 ($R_1 = 1 \text{k}\Omega, R_2 = 2 \text{k}\Omega$) as shown in Fig. 11. $\varepsilon'$ is defined as the static inaccuracy of the OP Amp as follows.

$$\varepsilon' = 2|V_o| - |V_i|.$$  \hfill (1)

Here, $V_o$ denotes the output voltage of the inverting amplifier. When the gain is equal to 2, the inaccuracy $\varepsilon'$ for plus DC input voltages corresponds to $\varepsilon$ for minus input voltages in the SC amplifier. Conversely, the inaccuracy $\varepsilon'$ for minus DC input voltages.
Fig. 8 Power dissipation vs. OP-Amp switching duty ratio in the SC amplifier.

Fig. 9 Output voltage inaccuracy vs. OP Amp switching duty ratio in the SC amplifier.

Fig. 10 DC input voltage versus output voltage inaccuracy for the inverting amplifier.

Fig. 11 Configuration of the inverting amplifier with the DSB OP Amp.

Fig. 12 Output voltage inaccuracy vs. SC amplifier gain.

Voltages corresponds to $\varepsilon$ for plus input voltages in the SC amplifier. The inaccuracy $\varepsilon' = 0.054$ V for a plus DC input voltage of $0.5$ V is close to $\varepsilon$ ($\sim 0.06$ V) for an input of $-0.5$ V as shown in Fig. 9. While, $\varepsilon' = 0.062$ V for a minus DC input voltage of $-0.5$ V is close to $\varepsilon$ ($\sim 0.045$ V) for an input of $+0.5$ V as shown in Fig. 9. Thus, the slightly large $\varepsilon$ ($\approx 0.045$ V–$0.065$ V) of the SC amplifier is almost the same as the static inaccuracy $\varepsilon'$ of the DSB OP Amp. This shows that the slightly large $\varepsilon$ ($\approx 0.045$ V–$0.065$ V) of the SC amplifier is mainly due to the static operational characteristics of the OP Amp. Thus, the slight differences in the inaccuracies $\varepsilon'$ and $\varepsilon$ for the plus/minus $0.5$ V input signals are caused by the dynamic operation of the DSB circuit and sampling circuits. Though the nonlinearity total harmonic distortion (THD) of the OP Amp itself for the $0.0154$ V$_{p-p}$ input signal ($10$ kHz) was $5.9$ %, the THD of the inverting amplifier with the negative feedback element for a $1$ V$_{p-p}$ input signal ($10$ kHz), was only $0.32$ %. Therefore, the inherent nonlinearity of the OP Amp when used as an amplifier with the negative feedback element is extremely small. $\varepsilon'$ becomes also nearly $0$ V when the wide-band high-gain Diffet (Dielectrically isolated FET) input bipolar OP Amp with the open loop gain A of $120$ dB is used [13]. From these two investigation results, we can say that the slightly large $\varepsilon'$ of $0.05$ V–$0.06$ V is caused by the output signal decrease because of the poor gain characteristics of the DSB OP Amp.

From these simulation results, it is thought that the dynamic operational inaccuracy of the SC amplifier has been caused mainly by the limited open loop gain of the OP Amp. If the performance of the OP Amp is increased to a high gain, the characteristics of the SC amplifier are expected to improve.

Because several SC amplifiers are used in the form of different gains in the filters, the gain dependency of the accuracy is also important. Figure 12 shows the output voltage inaccuracy versus the SC amplifier gain $C_1/C_2$ at a $\phi_1$ sampling pulse width $T_{s1} = 50$ ns and $\Delta T = 10$ ns. Obviously, the inaccuracy $\varepsilon$ depends on the SC amplifier gain and as its gain increases, the inaccuracy increases nearly linearly. The inaccuracy $\varepsilon$ in the low gains is caused by the same phenomena as mentioned above.

5. Conclusions

A high-speed CMOS OP Amp with a dynamic switching bias circuit capable of processing video signals for decreasing its
dissipated power, was proposed. Through simulations it was shown that the OP Amp was able to operate at a 10 MHz dynamic switching rate and a dissipated power of 66% of continuous operation. This OP Amp was applied to the switched capacitor non-inverting amplifier with a gain of 2 and its 10 MHz high-speed switching operation, capable of processing video signals, was confirmed. By increasing the switching duty ratio to 70%, the power dissipation of the non-inverting amplifier decreased to 56% of normal operation. Furthermore, simulation results showed that the output voltage inaccuracy for an SC amplifier with a gain of below 2 was below 6.5% and mainly caused by the limited open loop gain of the OP Amp. By improving the performance of the OP Amp, the inaccuracy of the SC amplifier is expected to decrease.

This DSB CMOS OP Amp circuit configuration should be very useful for the realization of low-power wide-band signal processing ICs. Because the DSB circuit also has potential for the applicability to various kinds of OP Amp circuits with current sources for control and for the contribution to lowering their power consumption, its application filed should be wide.

References


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He received his B.E. degree in electronics from Chiba University in 1973 and his Ph.D. degree in electrical engineering from Tokyo Metropolitan University in 2000. Until 1992, he worked at NEC Corporation. Then he joined Tokyo Metropolitan College of Technology, whose name has been changed to Tokyo Metropolitan College of Industrial Technology in 2006, where he is currently a professor. His research interests include CCDs, display devices, high-voltage MOS ICs, magnetic sensing, optical sensing, and signal processing. He is each senior member of IEEE and IEICE.