Progress in Wafer Level MEMS Packaging

1. Introduction

The packaging of microelectricomechanical system (MEMS) devices is one of the most challenging parts of MEMS commercialization. MEMS devices typically comprise cavities, and free-standing or even out-of-plane microstructures, while integrated circuits (ICs) do not. Due to this major difference in nature between MEMS and IC, packaging for MEMS must allow space for actuator movement, let the sensing element be able to interact with the surroundings via a pathway, or provide a suitable ambient inside package to achieve higher sensitivity or better reliability. Each particular kind of MEMS devices requires more customized and dedicated solution than just a standard solution which aims at packaging for all MEMS devices.1),2) In addition to the aforementioned issues, the common requirements for developing a MEMS packaging include protection of fragile structures, formation of electrical interconnects, manufacturability and reliability. The huge markets of mobile phones and handheld devices for computing and amusement applications generate new high volume markets for MEMS microphones, inertial sensors and RF MEMS devices. All these applications require thin and small packaged devices. Wafer level package and wafer level chip scale package have been widely used in IC packaging industry. Vertical interconnects and stacking chips are deployed as cornerstone technologies of SiP (System-in-a-Package) solutions for mass production of some commercially available ICs. The concept of SiP solutions can actually help the MEMS packaging.3),4) While most of the SiP solutions are relied on wafer level approaches, wafer level approaches for enabling MEMS packaging also show advantages in many aspects. In this paper, the progress of wafer level MEMS packaging will be surveyed. Some research subjects in future will be discussed as well.

Basic wafer level MEMS packaging involves major technology challenges in terms of ways for forming wafer bonding and electrical interconnections, and requirement of hermeticity or vacuum. Wafer level approaches are preferred by MEMS packages, since approaches at this stage are considered as batch type processes and they typically protect the microstructures away from the potential damages during die separation step. Besides, the know-good-die testing, die marking and die separation can be conducted at wafer level. Most of packaging and assembly steps for MEMS devices after that can be realized by leveraging the existing techniques in IC packaging. Thereby the packaging cost of MEMS device is drastically reduced, while the packaging yield is increased apparently.

2. Wafer Bonding Approaches

The first kind of wafer level MEMS packaging technologies are the approaches based on wafer bonding technologies. Nowadays wafer bonding techniques can...
be classified into two major categories: Direct bonding and bonding with intermediate layer.

2.1. Direct Bonding

Si fusion bonding, Si–Glass anodic bonding and surface activated bonding fall in this category. By forming –OH groups on the opposing surfaces of two wafers and annealing the bonded wafers at relative high temperature, \( 1,000^\circ C \), the strong bonding strength contributed by the Si–O–Si bridging bonds formed at the bonding interface leads the Si fusion bonding to be a good approach to form MEMS wafers with initial internal cavity. This sort of bonded wafers is suitable for being the initial wafer with embedded micro-cavities for making sensors and micromirrors after further micromachining steps. The second approach is the anodic bonding in which it is a well-established industrial technology now and mainly used for making MEMS pressure sensors. The sodium-containing glass wafer and silicon wafer are cleaned extensively and brought into pressure contact inside a chamber. High voltage (>1 kV) and high temperature (>400°C) cause an irreversible bond to form between the wafers. Anodic bonding works well for bonding glass or glass coated Si-wafers with silicon and nitride coated Si-wafers. In the case of surface activation bonding, the substrates are pre-treated with oxygen plasma, hydration processes or other chemicals to increase the reactivity, and then brought into contact with or without external pressure and high temperature to form an irreversible bond. When the wafer surface is cleaned by using argon beam sputtering in high vacuum environment, silicon wafers can be bonded at room temperature.

2.2. Bonding with Intermediate Layer

In this category, eutectic bonding, glass-frit bonding, solder bonding, thermocompression bonding and adhesive bonding are the known technologies. Eutectic bonding deploys a thin gold layer as an adhesive layer to bond silicon wafers. The wafers coated with a thin gold layer are brought into contact at the temperature higher than Au–Si eutectic point, i.e., \( 363^\circ C \) for 2.65% Si in Au. The common practice is bonding at \( 370^\circ C \) for 15 min under 7 KN of applied force by using commercial available bonder tool. The wafer-level packaging based on a glass frit sealed interface between the MEMS wafer and a cap wafer has been a major technology for volume production of MEMS accelerometers in automotive airbag systems to realize hermetic sealing. This way is similar to the long-established approach of glass frit as a seal in conventional hermetic ceramic packages. The cap wafer is stenciled with a mixture of glass and binder, patterned to be the walls of each device cavity. Firing the stenciled wafer sinters the stenciled glass onto the cap wafer, forming the cavity walls. Then the glass cap wafer is aligned and thermo-compression bonded to the device wafer, the bonding condition typically requires temperature higher than 400°C with an applied pressure of 2 bars. However, the reliable sealing using glass frit requires relatively wider wall sealing pattern. It implies less gross dies per bonded wafer.

Eutectic Au–Sn solder has long been recognized as an approach offering superior high temperature performance, high mechanical strength, and fluxless soldering, since the melting temperature of its eutectic composition (Au–30at.%Sn) is \( 280^\circ C \). It has been widely used in optoelectronics and microelectronics industries. It is a reliable solution for packages comprise sealing of Kovar case to ceramic substrate. On the other hand, it is a concerned issue that large residual stress will be introduced when two bonded wafers with relatively large difference in coefficient of thermal expansion (CTE) for the case that these two wafers undergoing a process of large temperature difference. Low temperature soldering is developed to ease off this issue. In–Sn (50/50) solder as the bonding intermediate layer has been investigated for packaging of thermal sensors and infrared imaging sensors. The helium leakage rate less than \( 1 \times 10^{-8} \text{torr l/s} \) and tensile strength of 200 kg/cm\(^2\) for the bonding interface can be obtained for bonding temperatures of 150°C. Au–In–Ni intermediate layer material has been characterized for packaging thermal sensor array as well. This study revealed a thermocompression approach based on the cold-welding characteristic of indium. In a bonding chamber with forming gas environment, e.g. \( \text{N}_2 \sim 90\% \) and \( \text{H}_2 \sim 10\% \), the shear strength of bonding interface can be obtained as of 72 MPa for condition of bonding temperature of 195°C, time of 10 min and applied pressure of 8 MPa. This package shows post-bonding temperature stability up to 473°C. Most of the batch type techniques for preparing the solder pattern on wafers for bonding include stenciling, dip-coating, electroplating and evaporation/sputtering. The technical challenges of this process are the uniformity control of solder pattern, thickness and composition. B. H.
Stark and K. Najafi report a molding and transferring technology that provides a way to solve the above challenges. They reflowed the solder paste in cavities with accurate volume inside vacuum chamber so as to convert the solder paste to be discrete solder ball in each cavity. Then this solder mold was aligned and bonded with MEMS device wafer in vacuum. By bonding at 260°C for 2 h for Bi/Sn solder, it can achieve vacuum packaged cavity with 1.5 torr.18)

In addition to the above-mentioned wafer bonding technologies using intermediate layer for hermetic sealing, the last group is the polymer based adhesive bonding for non-hermetic and near-hermetic packaging. Two polymer materials with major research interests are SU-8 and Benzocyclobutene (BCB). SU-8 is an epoxy-based negative resist material from Microchem, USA, while BCB is from the Dow Chemical Co. BCB shows minimal outgassing, low moisture uptake and excellent electrical properties. In one process, as shown in Fig. 1, the BCB is spin-coated onto the capping wafer and photo-patterned to provide seal rings. After the cap wafer is bonded with device wafer, multi-step dicing is used to expose the bonding pad area and separate each die from the bonded wafer (Figs. 1b and 1c). As an example, the capped die can be die bonded and wire bonded on a PCB. Thereafter the whole packaging process is accomplished by a molding step (Fig. 1d). The bonded wafer after dicing and its close-up view are shown in Figs. 1e and 1f, respectively. The reflow characteristic of BCB during curing step allows the planar electrical signal feedthroughs passing through the bonding ring, while it maintains a good sealing. RF MEMS switch and FBAR (film bulk acoustic resonator) filter have been packaged by using BCB capping process.19),20)

On the other hand, we do not want residual BCB left inside deep cavities for wafers with high aspect ratio cavities, then we should not use spin-on step to prepare the BCB coating layer. Besides, we could not use the spin-on process to prepare the BCB coating layer on a wafer with free-standing structures. New process called as the contact printing method shows its advantage over spin-on technique. The contact printing method use viscous BCB as “ink” and using a soft cured BCB pattern as stamp to improve the bond strength of full-wafer adhesive bonding with patterned BCB as intermediate bonding layer. This technology was successfully demonstrated that the bond strength of samples has been improved by a factor of 2 in comparison with the data of conventional spin-on BCB bonding technique.21),22)

3. Wafer Level Encapsulation

The “wafer level encapsulation” method is known as an approach which comprises steps of using a sacrificial material to cover the MEMS device and a deposited thin film of tensile stress to encapsulate the MEMS device at the beginning, removing the sacrificial layer by wet etching or vapor phase etching through opening, and encapsulating this opening by depositing a thin film finally. In the case of encapsulating the opening in a thin film reaction chamber with vacuum, the sealed MEMS device can preserve the sealed cavity at low vacuum. This concept has been applied to achieve wafer level packaging for pressure sensors of capacitive sensing23),24) and of piezoresistive sensing (Figs. 2a and 2b)25) based on using LPCVD SiN film sealing, and for resonators by using polysilicon film sealing (Fig. 2c).26),27) This process is rather suitable for sealing the surface micromachined MEMS devices due to its perfect process integration. To enhance the durability and mechanical robustness of the encapsulation, 20 μm thick epitaxial Si layer is prepared by using Dichlorosilane at 1,080°C to seal the MEMS structure first, denoted as the cap layer in Fig. 2d. Then trenches are etched through the cap layer so as to allow the HF vapor etching to remove the refilled SiO2 and to release the MEMS structure, thereby the electrical conductive paths will be isolated.20,29) Finally a layer of LPCVD oxide is deposited on top of the cap layer in which it seals over the trenches. Since the
oxide deposition furnace is under vacuum, the parts are also under vacuum when sealed. After the sealing oxide is deposited, metal layer is deposited and patterned to form the electrical leads and pads. Since SiO₂ is a permeable materials to the ambient gases, the silicon nitride film or metal layer on top of the oxide seal location can extend the vacuum life of package. This sort of technology has been applied for commercial production of MEMS oscillators as shown in Figs. 2e and 2f. Recently a ultracompact encapsulated accelerometer with die size of 387 μm × 387 μm × 230 μm has been demonstrated by using this epitaxial Si encapsulation technology, as shown in Fig. 2g.

One advantage of using high temperature sealing process, i.e., the said epitaxial Si deposition, to enable the Si oscillators embedded inside a sealed vacuum cavity is that the absorbed molecules inside cavity will be removed during the high temperature sealing step, just like the hot baking treatment. Thus this newly released product exhibits excellent performance in terms of ultralow long-term drift of device features and good frequency stability against to temperature variation.

However, this high temperature epitaxial Si sealing process limits the material selection for MEMS devices. Some metals and low temperature oxides cannot sustain their materials characteristics in such a high temperature step. A 3-mask low-temperature electroplating process has been proposed as shown in Fig. 3. An electroplated 40 μm thick nickel film is prepared on sacrificial photoresist layer of several micrometer first (Fig. 3a.5). After the photoresist has been removed via access holes (Fig. 3a.8), the access holes can be sealed by sputtering a metal layer or melting Pb/Sn solder (Figs. 3a.9 and 3a.10). If the final sealing step is handled inside vacuum chamber, sealed vacuum of about 1.5 torr could be obtained. Figures 3b and 3c show the schematic drawing of a sealed pirani vacuum sensor and electroplated nickel thick film cap, respectively. One drawback of this process is the photoresist removing step may take several hours. Recently a novel encapsulation technique deploys a thermal decomposition step within temperature range of 180°C to 260°C to vaporize the sacrificial polymer via a permeable polymer overcoat in order to result an encapsulated cap made of the suspended polymer overcoat, as shown in Figs. 4b to 4d and 4f. The hermetic sealing can be realized by additional sputtered metal on top of polymer overcoat (Figs. 4e and 4g). Besides, sealed vacuum around 1 torr or less can be achieved by conducting the metal hermetic sealing step inside a vac-
uum chamber. There are several advantages of this technology, such as follows:

a) Low-temperature processing—It is suitable for the packaging of MEMS devices that are sensitive to high temperatures and thermally induced residual stress.

b) Low cost and simple packaging process—Both the sacrificial and the overcoat polymers can be made photosensitive. It does not require cap-to-wafer alignment or wafer bonding step.

c) High yield process—Thermal decomposition of the sacrificial polymer is used instead of etching, which is stictionless, structurally benign and easy to be controlled.

In summary, recent progress in wafer level encapsulation technology has proven itself as a versatile packaging approach and this technology can be extended to any devices that do not need direct physical contact with the ambient (i.e., accelerometers, gyroscope sensors, MEMS resonators, RF switch, varactor and filters). The footprint of MEMS package using this technology is always smaller than bonded cap approach. Since it does not need extra bonding ring area. Both planar and vertical interconnects can be realized in this technology.
4. Interconnects

The most common electrical interconnects are the planar electrical leads. They are typically prepared on the same side of MEMS wafer. Two major kinds of planar electrical leads have been known to us, i.e., the buried and surface leads. The buried leads could be heavily doped Si or metal silicide, e.g., AlSi, to form a low resistive path on silicon substrate. For the surface lead line process, Al alloy process used in microelectronics is a common solution for MEMS (Fig. 1). However, the Al may need to be changed into other materials which can sustain in high temperature process. Highly doped polysilicon is common used as lead line materials in the surface micromachining technology (Fig. 3b), and it can sustain in all kinds of high temperature wafer bonding processes using intermediate layer. It should be also noticed that polysilicon leads typically exhibit higher 1/f noise than metal leads. In some resistive type of MEMS sensors, polysilicon leads may not be a good choice.

Secondly, anisotropic wet etched Si v-grooves could be the through wafer vertical electrical vias when metal leads were sputtered or electroplated on the v-groove sidewalls. Due to the angle of v-groove, the footprint of the through wafer v-groove vias is relatively larger, as shown in Fig. 5a. Since the size of the through wafer v-groove vias is simply determined by the thickness of wafer. Using a thin device layer Si of a SOI (silicon-on-insulator) wafer, the v-groove vias can be shrunk to a very small area (Figs. 5b and 5c).

Thirdly, through wafer vertical holes of silicon and glass substrates can be created by using deep reactive ion etching (DRIE) or photo assisted electro-chemical etching. After forming the insulation layer based on thermal oxidation, CVD dielectric layer coating, or CVD parylene coating processes, the through wafer vertical interconnects can be formed by heavily doped polysilicon conformal deposition, metal sputtering, metal plating, or vacuum metal sucking and refilling. Combining the vertical interconnects with cavities on the cap wafer can provide an advantage of forming high density of interconnects and wafer level packaging via simple bonding step at the same time. In particular wafer level packaging using solder intermediate layer with reflow function is very suitable for this approach. Because the solder reflow step will mechanically and electrically enhance the connection between the vertical interconnects of cap wafer and planar electrical pads of MEMS wafer. As shown in the Fig. 6, this concept has been applied to vacuum sealing of accelerometer (Figs. 6a and 6b) and hermetically sealing of RF MEMS switch (Figs. 6c and 6d). Without using the high temperature thermal oxidation process, a novel low temperature process of making thick SU-8 dielectric isolation between Cu vertical interconnects and surrounding Si sidewall has been reported. It renders us the possibility of creating vertical interconnects on a wafer after MEMS devices or Al planar electrical leads have been prepared on the same wafer. Additionally the vertical interconnects are quite useful for SiP applications with high I/O counts. Figure 7a shows an analog IC is stacked on top of a digital IC, where an infrared image detector array chip is bonded on top of this analog IC as shown in Fig. 7b. This advanced infrared image FPA (focal plane array) demonstrates the state of the art results of SiP for sensor packaging. The SiP technology is considered as a promising approach to realize very tiny packages of sensor modules for wireless sensor network applications.

5. Conclusion and Future Outlooks

After a decade of research and commercialization effort, wafer-level MEMS packaging has proven to be a leading solution for MEMS packaging. In addition to
the package size, cost, and performance advantages, wafer-level MEMS packaging provides a way for enabling SiP type of ultra-compact and thin package of hybrid integrating MEMS, optoelectronics, signal processing circuits and even energy source together. The concept of Microsystem-in-a-package (µSiP) may properly describe this kind of packaging technology. Market demands in smart home, homeland security, environment monitoring and medical care will drive the µSiP technology to show commercial products in near future.

In addition to wafer bonding type of MEMS packaging based on BCB intermediate layer, a low cost near-hermetic package using a liquid crystal polymer (LCP) substrate, cap and sealing ring has been widely deployed for packaging CMOS image sensors nowadays. LCP is a thermoplastic polymer with barrier properties an order of magnitude greater than epoxy plastic materials. The permeability of LCP to water vapor and to oxygen is close to that of glass. Without using wafers contain etched cavities, thick LCP ring can just be the necessary spacing layer between two bonded wafers so as to provide enough room for motion of MEMS moving parts. Sealed LCP cavity can pass helium leak testing, i.e., MIL-STD-883E. However, this sort of testing may not be appropriate for polymer type of packages, because it measures only fine and gross leaks, without considering permeability and out-gassing. Although, LCP and BCB based MEMS packages cannot be considered as “hermetic” package. They could be cost effective MEMS packaging solutions for consumer electronics applications.

Some of these MEMS devices require a controlled atmosphere in the cavity or even vacuum packaged cavity. Wafer-level packaging of vacuum cavities brings the cost advantage of simultaneously sealing an entire wafer of cavities in vacuum. This eliminates the manufacturing inefficiencies and the costs of individual
“pump down and pinch off” for archaic metal or ceramic vacuum packages in the conventional vacuum packages. Wafer-level packaging based on direct bonding, metal intermediate layer bonding and metal sealed encapsulation may provide the low cost MEMS vacuum packaging solutions. However, if we want to maintain the high vacuum over long lifetimes, the materials and seals used must be leak-free, impermeable and not sources of significant out-gassing. The high ratio of surface-to-volume of these micro-cavities makes the maintenance of packaged vacuum degree even more difficult in the wafer-level MEMS packaging. These surfaces are reservoirs of adsorbed gases like oxygen, carbon dioxide and reactive gases. Plated metal surface is considered as major source of dissolved hydrogen in which it is a potential device-killer in some cases. Integrating getter film inside the packaged cavities may be a good solution to overcome these concerns for enabling wafer-level MEMS vacuum packaging.\(^40,44\)

On the other hand, the conventional standard of hermeticity test based on MIL-883E is invalid for cavity volume of less than 1,000 nL\(^3\). Currently people measure the wafer-level-vacuum-packaged MEMS device characteristics and calibrate the measured data with data derived for devices tested in a well-controlled vacuum chamber with known vacuum degree. MEMS resonator can let us to discriminate the vacuum degree from 0.1 torr to several tens torr.\(^33\) Pirani sensor or resistive type of thermal sensor with suspended membrane structure on v-groove may let us to measure the vacuum degree from ambient down to 0.1 torr,\(^45\) while vacuum degree of 4 m torr can be detected by using bolometer or resistive type of thermal sensor of surface micromachined membrane with tight gap between suspended membrane and substrate.\(^46\) It is also reported that Pirani sensors using proper read out circuits to delete the self-heating effect can allow us to measure the vacuum degree down to \(10^{-7}\) torr.\(^47\) Besides, more research effort is demanded to establish the external wafer level non-destructive characterization approaches for MEMS wafer level vacuum packaging. Thereby we may increase the testing speed and reduce cost.

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