Abstract

Presumably the 21st century will see an advanced information society in which multimedia equipment is in common use. One of the basic technologies that support MEMS (Micro Electro Mechanical Systems), a new idea called electronic systems integration for practical application of an integrated block in which many different elements including not only electronic circuits but also sensors and actuators are combined, using Si wafers as basic elements. With today’s MEMS, the problems of suppressing delay in signal transmission and heat generation are highlighted, and intensive investigations are being conducted on such methods as three-dimensional packaging to miniaturize low-resistance Cu trenches (Damascene) and low-permittivity layer insulation films and wires. The problem with wafer-level three-dimensional packaging is how to carry out wiring between upper and lower wafers at the time of stacking. In the past practice, stacked wafers were connected through inner bumps formed on the through-hole interconnections. However, the bumps had to be polished to make them uniform in height because they were difficult to form with a uniform height. In order to solve this problem, we developed a technology of wiring wafers to each other by the molten metal suction method after stacking them in several layers in the three-dimensional direction, i.e., we succeeded in connecting wafers without bumps. The purpose of the present paper is to introduce this technology.

Key Words: Bumpless, Molten Metal Suction, Water Glass, Optical Excitation Electropolishing, Electro-Capillary Effect

1. Introduction

In the process of making a micro electro mechanical systems (MEMS) block by stacking Si wafers effective for dissipation, prevention and dispersion of heat, in the three-dimensional direction, through-holes are made in the Si wafers first. Then, Boron (P⁺⁺) is diffused on the wall surfaces of the through-holes to form shield layers, and different functions are built in each wafer. The wafers are stacked and each of them is wired to the upper and the lower ones for signal transmission and reception. Finally, electrodes (outer bumps) through which wafers are connected to the printed circuit board are formed. First, we describe the “optical excitation electropolishing method (OEEM)” technology of forming through-holes of high aspect ratio (hole depth/hole size: 100) at high density (3500 holes/mm²). The OEEM is a method of making holes by partial polishing. To prevent the leakage of the gas enclosed in the elements in each of the stacked layers, it is necessary to make joint layers and through-hole inter-
connections excellent in gastightness. Therefore, we developed the "water glass bonding" technology of joining wafers at low temperature (80 degrees C, 30 min). It guarantees excellent gastightness and does not degrade the functions built in the wafers. As a great number of wiring holes are made in the wafers integrated by water glass bonding, we also developed the "molten metal suction" technology of filling these holes with metal at a time.

These three technologies are necessary for wafer-level three-dimensional packaging and can also be applied to the bumpless, three-dimensional self-package block having the packaging function in itself.

2. Experimental Procedure

In this experiment, N-type Si wafers grown by the magnetic Czochralski (MCZ) method were used. Both surfaces of the wafer were polished to reduce the wafer thickness to 525 μm and were mirror-finished with Miller index (100). The resistivity of the Si wafer was 8.0-12.0 Ω cm. These wafers were processed step by step as shown in Figure 1 to fabricate a bumpless, three-dimensional through-hole interconnection block. In order to form through-holes of high aspect ratio in each wafer by OEEM, phosphorus was heavily diffused over the bottom surface of the Si wafer to decrease the contact resistance between the Si wafer and equipment electrode (Cu anode in Figure 4). The diffusion layer was 2.2 μm deep, and the surface dopant density was 2.2 × 10^20 atoms/cm^2. The through-holes were 10 μm square and 525 μm deep, so the aspect ratio was 52.5.

To form a diffusion layer for shielding on the wall surface of the through hole, about 1.0 cm^3 of a liquid organic boron [PBF: 3M-23 (B,O = 1.2 wt%: viscosity = 23 cP)] was added dropwise to the wafer surface. The organic boron was sucked into the through-hole in a vacuum of 7.0 × 10^-2 torr. Then, boron was diffused (1100°C, O2, 30 min) to obtain a diffusion layer depth of 2.5 μm and a surface dopant density of 1.0 × 10^20 atoms/cm^2. The film thickness of SiO2 grown on the wall surface of the hole was 500 nm, and a dielectric breakdown voltage over 300 V was obtained.

Each through-hole interconnection element formed in the experiment has a total of 73 through-holes (Figure 2). The center of the element is in the form of a concave in which there are 49 through-holes. These center through-holes serve as through-hole interconnections for selective wiring such as crossing of wires, alignment of electrode positions, etc. On the surrounding, there are additional 24 through-holes that, after being refilled with metal, serve as through-hole interconnections for transmitting and receiving signals from the functional circuits placed above and below. Refilling with metal by the molten metal suction method is carried out in two steps. Only the center through-holes are refilled first.

In the experiment the wafer was set in a closed type molten metal suction equipment as shown in Figure 3. The injection cabin was evacuated to 5.0 × 10^-7 torr, and
Fig. 3 Schematic illustration of closed type molten metal suction instrument

The gate valve of the heater cabin having an indium solution bath was opened. The specimen was dipped in the indium solution bath heated to 210°C. One minute after, atmospheric pressure was restored by introducing N₂ gas into the equipment. Afterward, the equipment was pressurized to 2.0 kg/cm² by feeding N₂ gas continuously. The specimen was withdrawn from the indium solution bath while applying a voltage of +15 VDC to the specimen to decrease the contact angle (electro-capillary effect) between the wall surface and the indium used to refill through-holes, and was returned to the injection cabin. Then, the gate valve of the heater cabin was closed. After keeping in the injection cabin for 5 minutes, the specimen was checked to ensure that the remaining indium on the surface had solidified, and was then removed from the equipment.

Four Si wafers having refilled center through-holes were integrated by using low-temperature bonding. The water glass used in this experiment was a solution of sodium silicate (SiO₂=36%, Na₂O=18%), a product of Kanto Kagaku Co., Ltd. The water glass solution was diluted to 0.1 wt% with ultra pure water and centrifuged (20000 rpm, 3 hr), and the obtained supernatant solution was used as adhesive. A water-absorbing SiO₂ film (300 nm) was formed on one of the wafers to be joined, and both wafers were subjected to hydrophilization (NH₄OH:H₂O₂:H₂O=1:2:7, 85°C, 10 min). One of the wafers was coated with adhesive by spinning (7000 rpm, 30 sec), and both wafers were aligned by an aligner and temporarily fastened by lightly holding down the center of the upper wafer with tweezers. After that, the upper wafer was pressed by a rubber roll with a force of less than 800 gf. Both wafers were joined in an N₂ gas atmosphere at 80°C for 30 minutes. The adhesive strength was more than 300 kgf/cm² (hydrogen bonding), and the leak rate of the joint was 1.0×10⁻¹⁰ Pa·m³/sec, so the joint was gastight. Then, the remaining through-holes for signal transmission and reception on the periphery were refilled with metal by the above-mentioned method to obtain through-hole interconnections.

Finally, outer bumps were formed on the bottom surface of integrated wafers, using the solder paste printing method, in the following ways. At the center of the outer bump, a thick polyimide layer (PI post: 30 μm) was arranged and used as a buffer to relieve thermal and mechanical strains resulting from the difference in thermal expansion coefficient between the printed circuit board and Si wafer. A 20 μm thick Cu layer was electroplated after Ni(0.5μm) and Ni(0.5μm) were sputtered on the PI post. This Cu layer was provided to maintain the bump height constant. A solder paste was printed on the Cu layer and was formed into a ball under its surface tension by passing through a reflow oven. The formed bumps were 80μm diameter, 70μm high and 100μm pitch.

3. Key Technologies and Discussion

3.1 Optical excitation electropolishing technology

Figure 4 shows the cross section of the equipment employed for optical excitation electropolishing. A 2.5 wt% HF solution was used as electrolyte. The Si wafer in which through-holes were formed was used as anode and a Pt plate was used as cathode. V-ditches were formed in advance by anisotropic etching to perform selective electropolishing at the places of the Si wafer where through-holes were to be made. The hole size was determined by the length of one side of the V-ditch. The voltage applied
to both electrodes was about 1.0 V<sub>DC</sub>.

A mercury lamp was used as the light source to irradiate the bottom surface of the wafer, and a band-path filter, which passes lights of wavelengths between 370 and 750 nm, was placed in the optical path. Positive holes as minority carriers are produced within a depth of about 11 µm from the bottom surface irradiated, and are made to move toward the surface of the Si wafer by the electric field applied to the system. If an acute-angled "defect" (V-ditch) exists on the surface of the Si wafer, the electric field concentrates at the acute-angled portion, causing electric charges (positive holes) to converge on it. Chemical reaction as shown below occurs there, and only that portion is etched to form a hole.

\[
\begin{align*}
\text{2HF} & \rightarrow 2\text{H}^+ + 2\text{F}^- \quad (1) \\
\text{Si} + 2\text{F}^- + \lambda (+) & \rightarrow \text{SiF}_2 + \lambda (-) \quad (2) \\
\text{SiF}_2 + 2\text{HF} & \rightarrow \text{SiF}_4 + \text{H}_2 \quad (3) \\
\text{SiF}_4 + 2\text{HF} & \rightarrow \text{H}_2\text{SiF}_6 \text{ (dissolved)} \quad (4)
\end{align*}
\]

A photograph of the cross section of the formed through-holes is given in Figure 5. The hole size is 4.4µm in diameter and the wafer thickness is 480µm, so the aspect ratio is 109. The density of through-holes is 3500 holes/mm<sup>2</sup>, and the angle of their inclination to the normal line is less than 3 degrees.

N-type Si wafers grown by the MCZ method were used. Both surfaces of the wafer were polished and mirror-finished with Miller index (100). The resistivity of the wafer was 1.0-2.0 Ω · cm. The fabrication conditions were as follows:

- Current density: 12 mA/cm<sup>2</sup>
- Temperature of electrolyte: 45 degrees C
- Surfactant: 10 wt% C<sub>2</sub>H<sub>5</sub>OH
- Intensity of irradiation light: 100 mW/cm<sup>2</sup>

The growth rate of hole depth under these conditions was about 1.0 µm/min.

Immediately after the through-holes were made in the Si wafer, SiO<sub>2</sub> layer was formed on the wall surface of each hole. The film thickness of SiO<sub>2</sub> grown on the wall surfaces of the through-holes was 500 nm. This oxide film was used as an insulator between the metal put in the hole and the Si wafer. After that, circuits and other functions were built in the Si wafer.

3.2 Water glass bonding

If residual stresses exist on the joints in the process of fabricating a three-dimensional integrated block, it becomes impossible to fabricate the block with good accuracy because peeling or deformation results. To solve this problem Low-temperature bonding was selected. Much water glass is used as the solvent to solidify silica sand when making casting molds. Solutions of sodium silicate, ammonium silicate, aluminum phosphate, etc are available for water glass. Here we describe an example using sodium silicate (SiO<sub>2</sub> = 36%, Na<sub>2</sub>O = 18%) supplied by Kanto Kagaku Co., Ltd. This is highly viscous, milky white liquid that is well soluble in water. The leak rate after the bonding was completed, was 1 × 10<sup>-10</sup> Pa · m<sup>3</sup>/sec when the caps of 0.32 mm seal width were joined (Figure 6). Moreover, eight 4-inch Si wafers, for example, could be joined. However, it should be noted that a water-absorbing porous film such as SiO<sub>2</sub> needs to be formed on one of the wafers to be joined to obtain a sponge effect.

3.3 Closed type molten metal suction method

In order to select a metal to refill through-holes, several metals were investigated based on the following criteria:

1. Melting point below 400°C for protection against degradation of the built-in functions on the Si wafer,
2. Low vapor pressure at the melting point to perform refilling operation in vacuum,
3. Low coefficient of thermal expansion to prevent the sucked metal from forming voids due to shrinking with temperature drop or coming out of the hole,
4. Low resistivity of metal to decrease electric resistance.

As a result, indium was selected. The closed type molten metal suction method was selected to refill through-holes with indium. A schematic view of the equipment used is shown in Figure 3.

Figure 7 is a photograph illustrating an unsatisfactory result of filling through-holes with metal (indium). As seen from the figure, the indium surface appears to be left at a position a little below the metal inlet, with the rest of indium torn off. Therefore, we concluded that indium...
dropped out by its own weight. The reason for it may be due to the fact that the contact angle of indium with respect to the insulation film (SiO$_2$) on the wall surface of the hole was so large that indium failed to enter into the irregularities on the wall surface completely, reducing in the contact area between SiO$_2$ and the wall surface. The solution to this problem is to decrease the contact angle with respect to SiO$_2$.

As shown in Figure 8, the interconnection has a MOS structure consisting of In, SiO$_2$, and Si. If a voltage is applied to between In and Si, the charge distribution varies due to the presence of mobile charges in the insulation film. The contact angle seems to vary depending on the amount of charges existing in the interface between indium and insulation film (electro-capillary effect).

Figure 9 shows the voltage dependence of the contact angle measured. The following can be seen from the figure:

1. Between -2.0 and 1.5 V, the contact angle increases with an increase in voltage, irrespective of the temperature of molten indium.
2. From 1.5 V to 15.0 V, the contact angle decreases where the higher the temperature of indium, the larger the decrease in the contact angle. At 340°C, the contact angle varied from 130 to 97 degrees while in the vicinity of 240°C, the contact angle change was small.

Due to the electro-capillary effect, it seems that indium does not drop out from deep capillaries when filled at 340°C. Surface tension can be calculated by the following equation:

$$\sigma = \rho \cdot g \cdot h^2 / 2 \cdot (1 - \cos \theta)$$

where $\sigma$ is the surface tension, $\rho$ is the density of indium, $g$ is the acceleration of gravity, $h$ is the depth of deep capillary, and $\theta$ is the contact angle. Assuming that the depth of deep capillary $h$ is 500 $\mu$m and the contact angle $\theta$ is 97 degrees, then the surface tension $\sigma_{\text{el}}$ is 8.54 g/sec$^2$ and the surface tension without applying electric field, $\sigma_{\text{no}}$, is 5.14 g/sec$^2$. Therefore, it seems clear that the surface tension increases by about 60% due to the electro-capillary effect.

The contact angle is greatly affected by the surface contamination and orientation of Si substrate and charges in the SiO$_2$ surface being in contact. In the SiO$_2$ film made carefully, there exist mobile charges and interface state due to the unavoidable inclusion of impurities such as the operator's sweat, chemicals, etc. The interface state in the SiO$_2$-Si interface contains positive charges because it has resulted mainly from oxygen vacancy. The interface state does not move under external voltage, but does affect the charge distribution in SiO$_2$ as it traps negative charges. By applying a positive voltage to the indium side, those mobile charges in SiO$_2$ which exist in the In-SiO$_2$ interface are made to move to the distant SiO$_2$-Si interface. That is, the reason for the decrease in contact angle in the In-SiO$_2$ interface may be due to the fact that the effect on the contact angle was reduced by moving the mobile charges far apart from the surface in contact with metal. Figure 10 shows a photograph of three-dimensional wiring formed by filling metal using electro-capillary effect.
4. Application of Key Technologies

When making a three-dimensional integrated block by joining wafers, it is necessary to concurrently connect the electrodes of each wafer. So far, the electrodes have been connected to each other through inner bumps. However, the use of bumps is disadvantageous in that it is difficult to make them uniform in height, and that the electrode connections become “open.” In addition, the gastightness of the joint cannot be obtained due to melting of the bump metal by the heat applied to join the wafers.

We have proposed a three-dimensional integrated block comprising Through-Hole Interconnection Chips (THICs) interposed between wafers having built-in functions (Figure 2,11&12). In the fabrication of this block, sensor elements and integrated circuit elements were manufactured at different plants, and THICs were interposed between the elements that have electrodes varying in location and function, followed by aligning the electrodes. Such THICs were integrated by water glass bonding into the three-dimensional (four-layer) block. Afterward, the through-holes were refilled with metal by the closed type molten metal suction method to carry out wiring of the three-dimensional integrated block. The wiring trenches (damascene-like) in the integrated circuits which required low resistance were, of course, refilled with metal and wired. The metal inlets on the bottom surface of the integrated block were sealed with a sputtered film of Cr (50 nm) and Cu (1000 nm) to prevent the metal from melting out by the heat applied in the post treatment process. The outside dimensions of this block were 2.5 mm by 2.5 mm by 2.0 mm, and the weight was about 10.0 mg. The maximum electrode length was 73.2 mm, the electric resistance was less than 278 Ω, and the capacitance was less than 160 pF. In this technology, double-sided IC wafers with both sides wired by through-hole interconnections are integrated by water glass bonding as shown in Figure 1. Then, all through-holes are refilled with metal at a time by the molten metal suction method. By doing so, a pre-assembled wafer-level three-dimensional integrated MEMS block is formed. This integrated block can be called “self-package type block” as it has the following packaging function:

1. Protection circuit elements against mechanical breakage,
2. Enabling every layer to enclose different type of gas,
3. Preventing disturbance from the outside of the block.

5. Conclusion

Success in the forthcoming age of multi-media equipment will depend on how to process much information in
a short time. With regard to semiconductor devices and microelectronics packaging to support such information processing, it will be very important to accomplish ultra-high-density integration (three-dimensional integration) and miniaturization of wiring. In this paper, we introduced three constituent technologies:

1) Optical excitation electropolishing technology of forming through-holes
2) Low-temperature water glass bonding technology that ensures high gastightness
3) Molten metal suction method that makes it possible to accomplish bumpless three-dimensional wiring at a time and showed that ultra-high-density three-dimensional packaging at wafer levels is feasible.

In addition, the integrated block using these technologies can ensure the excellent gas tightness and protects the built-in functions against disturbance and mechanical shocks (self-package structure).

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