A Design Method of Compact Lumped-Element Matching Circuits for Diplexers Using SAW Filters

Shinpei Oshima*, Tomonori Oshima*, Takuto Numao*, and Koji Wada**

*National Institute of Technology, Oyama College, Oyama, Tochigi 323-0806, Japan
**Graduate School of Informatics and Engineering, The University of Electro-Communications, Chofugaoka, Chofu, Tokyo 182-8585, Japan

(Received October 23, 2017; accepted September 29, 2018, published November 27, 2018)

Abstract

In this paper, a design method of compact matching circuits based on lumped elements for diplexers is proposed. This method only uses four elements for impedance matching of a common port and it is not required to modify a part of the filters. It is useful for fabricating compact diplexers on a printed circuit board. It can be applied to the diplexers with a wide band gap between two passbands. A prototype diplexer is designed. It is used as a receiver of the wideband code division multiple access Band 5 and the global positioning system. The diplexer achieves a compact size (8 mm × 8 mm) and insertion losses are less than 2.0 dB in each passband.

Keywords: Matching Circuit, Diplexer, Chip Component, SAW Filter, Printed Circuit Board

1. Introduction

Multi-band wireless communications have been used worldwide. Diplexers, which can separate two different frequencies, are important circuits for wireless communication systems. They are required for handling various frequency bands, because there are a lot of specifications for the wireless communication systems such as smartphones, wireless local area networks, and global positioning system (GPS) receivers. Figure 1 shows a schematic of the diplexer. It can be composed of two bandpass filters (BPFs) and matching circuits which connect a common port and the BPFs. The matching circuits must achieve proper impedance matching at two pass bands. Various diplexers have been already developed. The planar type diplexers can be fabricated on printed circuit boards (PCBs) by using printed conductor patterns.[1, 2] In order to achieve a compact size and high attenuation, diplexers that use surface acoustic wave (SAW) resonators have been developed.[3–6] Diplexers based on low temperature co-fired ceramic (LTCC) technology are useful for a compact size and low insertion losses.[7, 8]

Many planar diplexers use transmission lines for the matching circuits.[1] An open stub can also be used for the impedance matching.[2] These methods require relatively large areas on the PCB. A SAW duplexer which uses the matching circuits based on lumped elements was developed.[3] In [4] and [5], the SAW duplexers’ filters included a part of the function of the matching circuits. However, the bands of these SAW duplexers require a relatively narrow gap, due to the separation of the transmitted and received signals. The compact SAW duplexers are package type and the frequency bands are specified by manufactures.[6] Matching circuits based on LTCC technology have also been reported.[7, 8] In [8], the matching circuits of the wideband diplexer consist of three lumped elements. This diplexer is designed by modifying the three elements and a part of the filter for impedance matching. However, design procedures and a selection method of compact matching circuits were not investigated in detail. We therefore developed a compact matching circuits design method for the diplexers with a wide band gap between two passbands.[9–12]

In this paper, we describe in detail a compact lumped-
element matching circuits design method for SAW diplexers. The method only uses four lumped elements and it is not required to modify the design of the BPFs. It can be applied to the diplexers with a wide band gap between two passbands. It is suitable for the compact diplexers which consist of commercial filters and components on the PCB. In this study, the frequency bands require a receiver (Rx) of the wideband code division multiple access (W-CDMA) Band 5 (869–894 MHz) and the GPS (1574.42–1576.42 MHz). Unbalanced ports of Port 1 and Port 2 are 0.02 S. A balanced port of Port 3 is 0.01 S. In Section 2, the compact matching circuits design method is described. The diplexer for the W-CDMA Band 5 Rx and the GPS is also designed using the presented method. In Section 3, the frequency characteristics of the fabricated diplexer are evaluated in order to verify the effectiveness of the method.

2. Design Method of Compact Matching Circuits

Figure 2 shows a design procedure of the matching circuits. At first, input admittances of the SAW filters are measured and the compact matching circuits are selected. Then, by using equivalent circuits of the SAW filter with the matching circuit, equations for the design of the matching circuits are made. Values of the ideal lumped elements are determined by the equations. Finally, the frequency characteristics are verified by simulations. The details of the design procedure are described later.

Figure 3 shows the SAW filters’ input admittances for the GPS (FAR-F6KA-1G5754-L4AJ, TAIYO YUDEN CO., LTD.) and the W-CDMA Band 5 Rx (FAR-F5KB-881M50-B4ED, TAIYO YUDEN CO., LTD.). Note that the output port of the SAW filter for the W-CDMA Band 5 Rx is a balanced port. The size of the SAW filters is 1.4 mm × 1.0 mm × 0.5 mm. The input admittances are almost the reference admittance $Y_0$ (0.02 S) at the center frequencies of each filter. It should also be noted that the input admittance of the filter is in the capacitive region at the center frequency of the other filter. In this study, the matching circuits use the lumped elements for the compact size. Figure 4 (a) shows a schematic of the matching circuit (Type A). It is composed of a grounding inductor and a series capacitor. On the other hand, Fig. 4 (b) shows a schematic of the matching circuit (Type B). The type B matching circuit consists of a grounding capacitor and a series inductor. By using the matching circuits, the real part of the input admittance can set the reference admittance $Y_0$ and the imaginary part of the input admittance can be set arbitrarily. This method is based on the matching conditions using arbitrary susceptances.[7]

Figure 5 shows a plot of the input admittance of the SAW filter, with the matching circuits at the center frequency. This example assumes the Type A matching cir-
circuit as shown in Fig. 4 (a). $Y_{inA}$ moves to the inductive region, as shown in Fig. 5 (a), by means of the grounding inductor. The series capacitor can vary $Y_{in}$ as shown in Fig. 5 (b). As a result, as shown in Fig. 5 (c), the matching circuit adds an arbitrary susceptance to the reference admittance. The Type A matching circuit moves the input admittance counterclockwise in the stopband. The Type B matching circuit can also add an arbitrary susceptance to the reference admittance at the center frequency and can move the input admittance clockwise in the stopband. Generally, the matching circuits of the diplexers are designed at the center frequencies of each filter. Therefore, matching conditions in the low admittance region are suitable for good return losses at both edges of the passbands. In this study, the input admittance of the filter is in the capacitive region at the center frequency of the other filter, as shown in Fig. 3, and the Type A matching circuit is selected. The Type A matching circuit is suitable for setting the low admittance region with a relatively small phase shift.

Figure 6 shows a schematic of the diplexer for the W-CDMA Band 5 Rx and the GPS. It is composed of two SAW filters and the Type A matching circuits. Equivalent circuits at each center frequency are useful to derive the matching conditions.[13] Figure 7 shows the equivalent circuits of the SAW filter with inductance $L_1$ and capacitance $C_1$ at each center frequency. The passband of this SAW filter is the band of the W-CDMA Band 5 Rx. Here, $f_1$ and $f_2$ are center frequencies of the W-CDMA Band 5 Rx (881 MHz) and the GPS (1575 MHz), respectively. $B_1$ is an input susceptance of the SAW filter for the W-CDMA Band 5 Rx at $f_2$, which is specified by the input admittance shown in Fig. 3 (b). Similarly, Fig. 8 indicates the equivalent circuits of the SAW filter with inductance $L_2$ and capacitance $C_2$ at the center frequencies. The passband of the SAW filter is the band of the GPS. $B_2$ is the input susceptance of the SAW filter for the GPS at $f_1$, which is specified by the input admittance shown in Fig. 3 (a). The matching conditions are given by the following four equations. Here, $Y_{1p}$, $Y_{2p}$, $Y_{1o}$ and $Y_{2o}$ are the input admittances at the center frequencies as shown in Figs. 7 and 8.

\[ \text{Re}\{Y_{1p}\} = Y_0 \quad \text{(at } f_1) \]
\[ \text{Re}\{Y_{2p}\} = Y_0 \quad \text{(at } f_2) \]
\[ \text{Im}\{Y_{1p}\} + \text{Im}\{Y_{2o}\} = 0 \quad \text{(at } f_1) \]
\[ \text{Im}\{Y_{2p}\} + \text{Im}\{Y_{1o}\} = 0 \quad \text{(at } f_2) \]

Fig. 5 Diagrams of input admittance with the matching circuit.

Fig. 6 Schematic of the diplexer for the W-CDMA Band 5 Rx and the GPS.

Fig. 7 Equivalent circuits for the W-CDMA side.

Fig. 8 Equivalent circuits for the GPS side.
Therefore, the following equations are obtained

\[
\frac{C_2^2 L_2 Y_0 \omega_0^4}{1 + L_2 \omega_0^2 \left\{ L_1 Y_0^2 + C_1 \left( -2 + C_1 L_2 \omega_0^2 \right) \right\}} = Y_0
\] (5)

\[
B_2 - \omega_1 \left( C_2 + B_2^2 L_2 \right) \frac{C_1 \omega_1 \left( 1 + L_1 \omega_0^2 \left( -C_1 + L_1 Y_0^2 \right) \right)}{1 + L_2 \omega_0 \left( B_2 + C_2 \omega_0^2 \right)} \]
\[
+ \frac{C_2 \omega_2 \left( 1 + L_2 \omega_0^2 \left( -C_2 + L_2 Y_0^2 \right) \right)}{1 + L_2 \omega_0 \left( B_2 + C_2 \omega_0^2 \right)} = 0
\] (6)

\[
\frac{C_2^2 L_2^2 Y_0 \omega_0^4}{1 + L_2 \omega_0^2 \left\{ L_1 Y_0^2 + C_1 \left( -2 + C_1 L_2 \omega_0^2 \right) \right\}} = Y_0
\] (7)

\[
B_1 - \omega_1 \left( C_1 + B_1^2 L_1 \right) \frac{C_2 \omega_2 \left( 1 + L_2 \omega_0^2 \left( -C_2 + L_2 Y_0^2 \right) \right)}{1 + L_1 \omega_0 \left( B_1 + C_1 \omega_0^2 \right)} \]
\[
+ \frac{C_1 \omega_1 \left( 1 + L_1 \omega_0^2 \left( -C_1 + L_1 Y_0^2 \right) \right)}{1 + L_1 \omega_0 \left( B_1 + C_1 \omega_0^2 \right)} = 0
\] (8)

where \( \omega_0 = 2 \pi f \), \( \omega_1 = 2 \pi f_1 \), \( B_1 = 0.03694 \) S, \( B_2 = 0.01201 \) S and \( Y_0 \) is set to 0.02 S in this study. Values of the four lumped elements \((L_1, L_2, C_1, \text{and } C_2)\) are determined by the equations. This numerical calculation to obtain approximate solutions is carried out by a commercial software (Wolfram Mathematica).

Table 1 indicates designed values of the matching circuits. Note that \( C_2 \) is very large in the high frequency region. The impedance of capacitance \( C_2 \) is \( j0.012 \Omega \) at 881 MHz and \( j0.007 \Omega \) at 1575 MHz. They are almost a short circuit condition. Figures 9, 10, 11, and 12 show results simulated by Advanced Design System (Keysight Technologies, Inc.) which is a commercial circuit simulator. These simulations are carried out by using ideal lumped elements and measured S-parameters of the SAW filters. Therefore, the lumped elements do not consider stray elements such as the equivalent series inductance. The simulated results do not include effects of the electrodes on the PCB. The simulations using S-parameters of the lumped elements and the SAW filters are carried out to perform a high-accuracy simulation. Table 2 shows the specifications of the chip components (TAIYU YUDEN CO., LTD.). These are selected based on the designed values shown in Table 1. Figures 13 and 14 show simulated results. In the simulations, the measured S-parameters of the SAW filters are used. The S-parameters of the chip components are provided by the manufacturer (TAIYO YUDEN CO., LTD.). The S-parameters of the chip components include

<table>
<thead>
<tr>
<th>Table 1</th>
<th>Values of matching circuits.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( L_1 )</td>
</tr>
<tr>
<td>---------</td>
<td>-----------</td>
</tr>
<tr>
<td></td>
<td>11.12 nH</td>
</tr>
</tbody>
</table>

Fig. 9 Simulated results of S-parameters \((S_{ds31}, S_{ss11})\).

Fig. 10 Simulated results of S-parameters \((S_{ds21}, S_{ss11})\).

Fig. 11 Simulated result of S-parameter \((S_{ds32})\).

Fig. 12 Simulated results of S-parameters from 0.5 GHz to 2.5 GHz.
stray elements of the chip components. These results confirm that the frequency characteristics agree well with the simulated results as shown in Figs. 9 and 10.

3. Experiment

Experiments are carried out to verify the presented method. The PCB is made of FR4 and the substrate is 0.5 mm thick, with conductors on the top and bottom. The conductor patterns are connected by several through holes. The diameter of small through holes which are located near surface mount components is 0.3 mm. The diameter of large through holes is 0.5 mm. Conductors are made of copper. Figure 15 shows the conductor patterns which are for the surface mount components. Specifically, the lengths of the patterns are less than 1.4 mm. Figure 16 indicates a simulation model of the conductor pattern and

Fig. 15 Top view of the conductor patterns of the diplexer.

Fig. 16 Simulation model of the conductor pattern.

Fig. 17 Simulated results of conductor pattern as shown in Fig. 16.

Fig. 17 shows the simulated results of an electro-magnetic simulator. This simulation is carried out by the commercial electro-magnetic simulator Femtet (Murata software Co., Ltd). The relative permittivity and tanδ are assumed to be 4.7 and 0.013, respectively. It is confirmed that the return loss is less than 11 dB. Figure 18 shows a photograph of the prototype diplexer. The top layer has solder resists to mount the chip components and the SAW filters. The design area of the diplexer is less than 8 mm × 8 mm. Figure 19 shows a photograph of a measurement system using probes. The diplexer is measured by a network analyzer (Agilent Technologies E5071C) and a probe station system (Cascade Microtech MPS150). The probes are a
The measurement system using the GSG probes is calibrated with the impedance standard substrate (Cascade Microtech 106-682). Figures 20, 21, 22 and 23 show the frequency characteristics of the prototype. Table 3 shows the characteristics of the diplexer with targeted insertion losses and attenuations. The insertion loss at the band of the W-CDMA Band 5 Rx is less than 2.0 dB and that at the band of the GPS is less than 1.5 dB. Isolation is higher than 48 dB. The targeted amplitude difference is within ±1.0 dB and the targeted phase difference is within ±1.0 degrees.

Table 3. Measured results.

<table>
<thead>
<tr>
<th>Item</th>
<th>Frequency [MHz]</th>
<th>Target [dB]</th>
<th>Measured [dB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Insertion loss</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(S_{ds31})</td>
<td>869–894</td>
<td>&lt;2.5</td>
<td>&lt;2.0</td>
</tr>
<tr>
<td>Attenuation</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(S_{ss31})</td>
<td>500–824</td>
<td>&gt;50</td>
<td>&gt;63</td>
</tr>
<tr>
<td></td>
<td>824–849</td>
<td>&gt;45</td>
<td>&gt;55</td>
</tr>
<tr>
<td></td>
<td>914–960</td>
<td>&gt;25</td>
<td>&gt;34</td>
</tr>
<tr>
<td></td>
<td>960–2000</td>
<td>&gt;40</td>
<td>&gt;51</td>
</tr>
<tr>
<td>Insertion loss</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(S_{ds21})</td>
<td>1574.42–1576.42</td>
<td>&lt;2.0</td>
<td>&lt;1.5</td>
</tr>
<tr>
<td>Attenuation</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(S_{ss21})</td>
<td>500–1476</td>
<td>&gt;40</td>
<td>&gt;41</td>
</tr>
<tr>
<td></td>
<td>1476–1526</td>
<td>&gt;37</td>
<td>&gt;44</td>
</tr>
<tr>
<td></td>
<td>1625–1980</td>
<td>&gt;41</td>
<td>&gt;48</td>
</tr>
<tr>
<td></td>
<td>1980–2500</td>
<td>&gt;35</td>
<td>&gt;49</td>
</tr>
</tbody>
</table>

ground-signal-ground (GSG) type (Cascade Microtech ACP40). The measurement system using the GSG probes is calibrated with the impedance standard substrate (Cascade Microtech 106-682). Figures 20, 21, 22 and 23 show the frequency characteristics of the prototype. Table 3 shows the characteristics of the diplexer with targeted insertion losses and attenuations. The insertion loss at the band of the W-CDMA Band 5 Rx is less than 2.0 dB and that at the band of the GPS is less than 1.5 dB. Isolation is higher than 48 dB. The targeted amplitude difference is within ±1.0 dB and the targeted phase difference is within ±1.0 degrees.
$180 \pm 10^\circ$ at the passband of the W-CDMA Band 5 Rx. The measured amplitude difference is within 0.3 dB and the phase difference is within $180 \pm 4^\circ$. These values satisfy the target characteristics. The diplexer achieves high attenuation performance from 0.5 GHz to 2.5 GHz. Table 4 shows a comparison with other experiments. The prototype diplexer developed in this work, had a compact size compared with the planar diplexers in [1] and [2], and it successfully separated the bands, assuming a wide band gap. Furthermore, the method did not require any filter design.

### 4. Conclusion

A design method for a compact diplexer using SAW filters and chip components has been presented. This method applies four lumped elements for the matching circuits. It is suitable for the compact diplexers which use the commercial filters and components. It can be applied to the diplexers with a wide band gap between two passbands. The diplexer for the W-CDMA Band 5 Rx and the GPS is designed by using the presented method. The prototype achieves low insertion losses and high-isolation performance. The measured results are in good agreement with the simulated results. In the near future, we will study the elements sensitivity of the matching circuits. We also plan to design diplexers which can be applied for various specifications by means of the presented method.

### Acknowledgment

Authors would like to thank Keysight Technologies, Inc. for support of simulation technology. We also wish to thank TAIYO YUDEN CO., LTD. for the offer of chip components.

### References


-electronics filters, and SAW filters. This study focuses on the design of a diplexer using planar BPFs and lumped element matching circuits.

Appendix

In this study, the diplexer has the balanced port of Port 3. Therefore, the frequency characteristics of the diplexer are evaluated by the mixed-mode S-parameters. The mixed-mode S-parameters are given by:

\[
S_{ss11} = S_{11} \quad (A.1)
\]

\[
S_{ss21} = S_{21} \quad (A.2)
\]

\[
S_{ds31} = \frac{(S_{A1} - S_{B1})}{\sqrt{2}} \quad (A.3)
\]

\[
S_{ds32} = \frac{(S_{A2} - S_{B2})}{\sqrt{2}} \quad (A.4)
\]

In this case, Port 3 consists of Port A and Port B which are unbalanced ports. \(S_{ss11}\) is the return loss of the common port. \(S_{ss21}\) is the insertion loss between Port 1 and Port 2. \(S_{ds31}\) is the insertion loss between Port 1 and Port 3. \(S_{ds32}\) is the isolation between Port 2 and Port 3.