IMB Technology for Embedded Active and Passive Components in SiP, SiB and Single IC Package Applications

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Abstract

There is a strong development activity constantly ongoing in the electronics packaging industry to find new and cost-effective packaging solutions. At the same time that existing package technology solutions are being pushed to the limit, completely new and revolutionary electronics manufacturing solutions are emerging to the market. A great challenge in the ongoing development is to be able to create a package technology solution that provides further miniaturization and improved electrical performance with a cost effective and robust manufacturing concept.

Imbera Electronics has developed several generations of Integrated Module Board (IMB) technology to embed discrete components inside an organic, low-cost PCB motherboard or substrate. The 1st and 2nd generations were initially developed in late 90's at the Helsinki University of Technology. The current focus is in the 3rd generation IMB technology developed by Imbera Electronics in 2003. The 3rd generation technology provides a flexible platform for multiple component types from low- to mid-range I/O count components.

In this paper the IMB technology concept is reviewed with a focus on technology capability, reliability, production quality and potential application areas. The cost impact of different production process alternatives are studied and reviewed. Also, an analysis of key cost drivers is presented.

Keywords: IMB, Integrated Module Board Technology, Embedded, Active, Passive, Miniaturization, PCB, Printed Circuit Board, Integration, Reliability

1. Introduction

Today's mobile handset market is driving the development of novel technology solutions to improve product performance, shrink the form size and still maintain low total cost of ownership. One of the current package solutions has been to stack components in 3D format utilizing wire-bonding or soldering techniques. However these solutions have limitations and thus the industry is in search of new packaging technologies to further improve the product performance and miniaturization.

Embedding components inside a PCB motherboard or a substrate provides literally a new dimension to achieve the needs of today's high end electronics manufacturing. Component embedding inside a substrate is not a completely new idea, and several technology approaches have been in development over the years – the first real attempt to commercialize an embedding technology was done by GE in mid 80's.[1] But only now has the market evolved to accept

component-embedding solutions and at the same time the infrastructure has matured to a level where component embedding becomes a commercially viable solution.

2. Imbera IMB Technology Solution

Imbera Electronics has worked in the area of embedded components since 2002. The technology development itself was started at the Helsinki University of Technology in 1997.[2] Over the years Imbera has developed and evolved several technology concepts for component embedding. The current 3rd generation Integrated Module Board (IMB) technology solution provides a robust, flexible and a cost effective process for component embedding.

The 3rd gen IMB technology is feasible for embedding low- to mid-range I/O count components, with the main target area of components in the range 2 to 350 I/Os. The technology has been proven for Si, GaAs, IPD, and discrete C and R components. Figures 1, 2 and 3 show typical

IMB module level products with one embedded silicon component. iQFN represents a low pin-count product area with only one conductor layer, iBGA has a higher routing capability through multiple conductor layers, and the standard IMB module has one embedded component inside a standard interposer and one wire bonded component on top (with over-mould). The iQFN package has one conductor layer that is used for both die to package electrical interconnection and solder lands. The layer has good level of freedom to support typical interconnection structures, and can replicate a standard QFN solder-land layout. The iBGA package has full freedom in solder-land design and supports, for example, a full array BGA layout structure. Requirements for the standard IMB module are similar to typical interposers and both the upper and lower surfaces support normal package designs. Furthermore, all module structures support multiple embedded components that can be assembled side-by-side or stacked.

IMB technology production utilizes standard, widely available materials and processes. This enables a large supply base and competitive total cost of ownership.

The IMB manufacturing process is presented in Figure 4. The process begins with a metal foil onto which microvias and alignment marks are drilled with a laser.

Fig. 1 iQFN for sub 100 I/Os.

Fig. 2 iBGA for sub 350 I/Os.

Fig. 3 Standard IMB module for sub 350 I/Os.

Non-conductive paste (NCP) is printed onto the foil and passive and/or active components are assembled using a chip shooter or flip chip bonder. A minimum of 3 μm copper or gold metallization is required on the component pad openings. Typically the components are assembled with a chip shooter due to its faster processing time, which helps to minimize the cost of embedding. After the components are assembled and the NCP is cured, the PCB core is manufactured around the components using standard pre-preg materials. The pre-preg has pre-manufactured openings in the area of the embedded components. Material can then be selected based upon the product requirements (normal FR-4, high Tg FR-4, or BT epoxy). Once the pre-preg is cured with a PCB pressing machine, the copper foil is patterned to form the desired routing layer. Several PCB process flows can then be selected based upon the product requirements. In the motherboard applications, the manufacturing is typically done using a minimum 50 μm L/S process. With more advanced structures - such as iBGA - a semi-additive process can be used to achieve a 30 μm L/S process or below. In substrate applications the maximum layer count is normally limited to 6 in order to secure high yields. A typical layer count in motherboard applications is from 8 to 10.[3, 4]

Fig. 4 Integrated Module Board process flow (4-layer substrate with embedded active and passive).

Fig. 5 Embedded die interconnection area (polymer layers selectively removed).

Figure 5 presents a top view of the embedded die after the polymer layers have been selectively removed. The I/O structure is staggered to several rows in order to provide sufficient tolerance for the chip shooter machine and PCB processes.

3. IMB Application Areas

IMB application areas are presented in Table 1. The technology can be utilized in both motherboard and module types of products. For low-cost packaging the component module contains routing layers only on one side of the module.

The technology provides a flexible and robust platform for various component types. The technology does not have any thickness restrictions and can be used with standard discrete passives, IPD, Si, and GaAs components. The embedded core is typically less than 250 μm in thickness, with component thicknesses from 50 μm to 150 μm . In order to fabricate a reliable 3rd generation IMB interconnection, the component needs to have a minimum of 3 μm copper or gold plating. Future IMB technology will enable a bumpless interconnection with metallization thickness below 1 μm .

4. Reliability Evaluation

An iQFN product with one conductor layer was selected

to verify the IMB technology reliability. The package has one wiring layer connecting the component I/Os to the package pins (28 pieces), and a standard QFN solder pad layout for external connection. The pad pitch is 0.5 mm and OSP coating covers the pad areas. The package design enables very good manufacturability and high yields in manufacturing. Industry standard reliability specifications were used to determinate the package and board level reliability. The test methods used are shown in Table 2.

The tested package has a 2.13 mm $\times$ 2.13 mm daisy-chain test silicon die embedded inside a 4.0 mm $\times$ 4.0 mm package. The embedded component thickness is 150 μm and the full package thickness is 340 μm . A 50 μm /50 μm L/S PCB process was selected for manufacturing the interconnection layer. The component was assembled with a chip shooter machine; ± 13 μm alignment accuracy, 7000 UPH. The final electrical yield of the product was 99.35%.

Figure 6 presents a cross sectional schematic presentation of the iQFN package structure. The package has one embedded component and one conductor layer. The same conductor layer forms the electrical interconnection with the embedded component and with the motherboard.

A summary of the reliability tests is presented in Table 2. Typical JEDEC standards used in consumer electronics were selected to verify the reliability of the iQFN package. Both package and board level tests were selected to

Table 1 IMB application categories.

	System in Board (SIB)	System in Package (SIP)	Low Cost Package

Description	Embedded components inside a PCB motherboard. » <i>miniaturization</i> » <i>excellent electrical performance</i>	Embedded component inside a component interposer. » <i>miniaturization</i> » <i>excellent electrical performance</i> » <i>excellent thermal performance</i> » <i>embedded EMI shield</i>	Escape routing only on one side of the package [structure resembles FC-BGA or fan out WLP] » One or more embedded components with the package (both active and passive).
Features	<i>High speed component assembly</i> » UPH typically 15000 or higher (only with chip shooter) Motherboard PCB processes » minimum L/S 50 μm /50 μm » maximum layer count 10	<i>Medium speed component assembly</i> » Chip shooter UPH typically around 5000 (down to ± 13 μm accuracy) » FC process user for higher accuracy alignment (UPH below 1000) Substrate PCB processes » minimum L/S 30 μm /30 μm » maximum layer count 8	<i>Low cost package solution</i> » minimized PCB costs/unit <i>Medium speed component assembly</i> <i>Motherboard or substrate PCB process</i> » maximum layer count 3
Embedded components	Medium low I/O count Si or GaAs » <i>up to 150–200 I/Os</i> Embedded passives; » resistors, capacitors, IPDs	Medium high I/O count Si or GaAs » <i>up to 300–350 I/Os</i> Embedded passives; » resistors, capacitors, IPDs	Low to medium I/O count Si or GaAs » <i>iQFN around 100 I/Os</i> » <i>iBGA around 300 I/Os</i> Embedded passives; » resistors, capacitors, IPDs

Table 2 iQFN test summary

	Test method	Standard (JEDEC)	Conditions	Result
Package Level	Reflow Moisture Sensitibe	J-ST D-020	Level 1 85°C/85% RH 168 h + reflow 3 times	pass
	Thermal Cycling	JES D22-A104	Condition: M (−40°C – +150°C) Soak mode 3 (10 min) Cycles per hour: 2 Cycle count: 500	pass
	Temperature Humidity Biss	JES D22-A101	Condition: 85°C 85% humid, 1000 h	pass
	High Temp Storage	JES D22-A103	Condition A: 125°C, 500 h	pass
	Low Temp Storage	JES D22-A103	Condition A: −40°C ± 3°C, 168 h	pass
Board Level	Mechanical Shook	JES D22-B104	B, 1500 G	pass
	Thermal Cycling	JES D22-A104	Condition: (−40°C – +125°C) Soak mode 3 (10 min) Cycles per heure. 2 Cycle count: 500	pass

Fig. 6 iQFN package structure.

ensure full coverage of potential failure mechanics in different environments. The iQFN package passed all the tests with no failures.

5. Cost Impact of Assembly and Bumping Technologies

Component assembly cycle time has a crucial role in the total cost of IMB production. Therefore, it has been important for Imbera to develop a fast component-attachment method to enable wider technology acceptance. These advanced mass-production methods improve the component-assembly process and replace traditional high-accuracy Flip-Chip assembly technology in the low-end and mid-range product areas.

An iBGA design with two conductor layers was chosen to demonstrate the cost impact of IMB technology in different manufacturing environments. The example

Fig. 7 iBGA package structure.

Table 3 Cost comparison of different component assembly technologies.

design is a $7 \times 7 \text{ mm}^2$ iBGA package with one build-up layer. The package includes $5 \times 5 \text{ mm}^2$ silicon component with 120 I/Os. A schematic diagram of the iBGA package is shown in Figure 7.

The three different attachment methods in this cost analysis use Flip Chip, chip shooter, and advanced chip shooter manufacturing techniques. The chip shooter has a capacity of 7000 UPH and the advanced chip shooter has a capacity of 15000 UPH, while the Flip-Chip bonder has a capacity of below 1000 UPH. The cost impact of the different chip attachment methods are presented in Table 3. iBGA assembled using the Flip-Chip bonder is indexed to be 100%. The cost of the alternative bonding technologies is presented relative to the iBGA assembled using the Flip-Chip bonder. Shorter assembly time significantly reduces the total cost of component embedding due to lower amounts of allocated depreciation and factory overheads. Also, the improved capacity significantly impacts the required facility and equipment investment needs.

In the assembly cost comparison, it can be noted that, by assembling the components with a chip shooter, the cost efficiency of IMB products can be improved by 20%. By optimizing the assembly process even further, costs can be reduced by 25% compared to iBGA products assembled with a Flip-Chip bonder.

Bumping of the embedded components is also an important cost factor. The bump is usually manufactured at the wafer level and the process includes several steps to form the desired metallization structure. Imbera 3rd gen IMB technology utilizes standard Au or Cu bumping techniques to manufacture an IMB-optimized bump structure. While

Table 4 Cost comparison of the wafer treatment.

embedding a standard Wafer Level Package (WLP) is technically possible, it is rarely used due to the significant cost increase.

A cost comparison of the three different wafer-level processes is presented in Table 4. These selected processes are WLP technology, an Imbera-specified copper-bumping process, and Imbera bumpless technology.

The cost comparison of the wafer-level processes shows that a remarkable cost saving is achieved by moving from current WLP technology to standard copper bumps. Imbera's next generation solution of bumpless technology is expected to provide an 80% cost savings in the iBGA product.

6. Conclusions

In this paper, recent advancements in IMB technology in various product areas were presented. Also, a study to verify the reliability of IMB technology was shown and a

sufficient reliability level was reported.

The cost of different assembly and wafer-level bumping technologies was studied. It was shown that a significant cost reduction can be achieved when moving from Flip-Chip assembled iBGAs to chip shooter technology (while still maintaining sufficient alignment accuracy for component placement). Also, it was shown that the cost of WLP increases the total cost of embedding and reduces the potential of the technology. Further, it was shown that a significant cost reduction can be achieved when adopting the bumpless IMB technology.

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